Serial-interface , Touch screen controller

Features

- Multiplexed Analog Digitization with 12-bit Resolution
- Low Power operation for 2.2V TO 5.25V
- Built-In BandGap with Internal Buffer for 2.5V Voltage Reference
- Temperature Measurement and Digitization
- Auxiliary Inputs for Measurement of Battery Voltage
- Low on-resistive MOS for sensing and switching
- Supports Interface for 1.5V to 5.25V Logic Levels
- Internal Power-On-Reset (POR)
- Standard Serial 3-wire Digital Data Interface
- Available TSSOP-16 and QFN-16 Packages

Applications

- Personal Digital Assistants
- Mobile Phones
- Smart Hand-held or Gaming Devices
- Touch Screen monitors
- Point-of-sale Terminals
- Digital Frame Devices
- GPS and Pagers

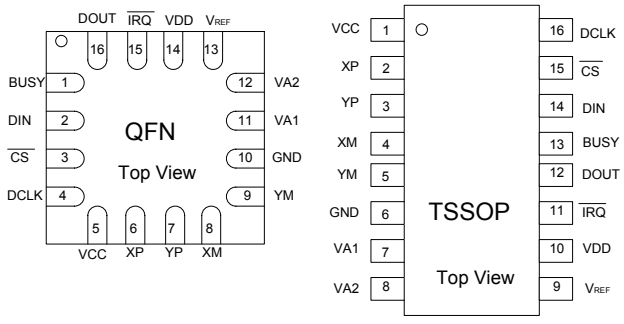
Description

The AUR3840 is a high-resolution analog sampling and digitizing integrated circuit supports industry-standard 4-wire touch screen control and host interface operations. The chip includes a 12-bit successive approximation analog-to-digital converter (ADC) with a synchronous serial interface and multiplexer-switcher circuits for flexible measurement of pressure sensitive voltage or other applicable analog voltages.

An accurate Bandgap reference voltage is built-in and associated with a temperature detection circuit for an on-chip digital temperature measurement. Two auxiliary analog inputs are also provided for digitization with the ADC. It could be applied for a direct measurement of system battery power supply voltage, or for smart power monitoring and management needs.

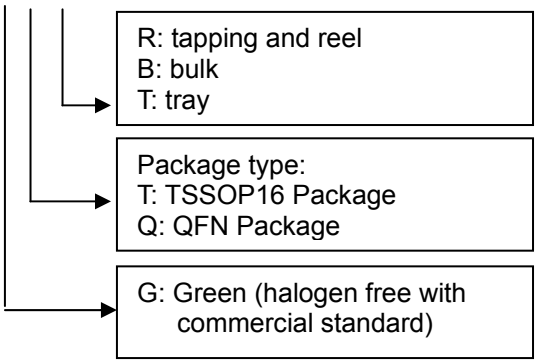
The on-chip 2.5V reference voltage buffer circuit is available to either internal or external usages, and can be turned off to save power. This low-power CMOS circuit integration with optimized low-current consumption provides an ideal choice for battery operated devices or systems for power saving and green operations. The AUR3840 is available in TSSOP-16 and QFN-16 packages and is specified over the temperature range of –40°C to +85°C

Package Information



Order Information

AUR3840☐☐☐



Pin Functions

TSSOP	QFN	Pin Name	PIN TYPE	Pin Function
1	5	VCC	POWER	Supply Voltage
2	6	XP	AI	XP Contact Pin
3	7	YP	AI	YP Contact Pin
4	8	XM	AI	XM Contact Pin
5	9	YM	AI	YM Contact Pin
6	10	GND	GROUND	Power Ground
7	11	VA1	AI	Battery Measurement Analog Input
8	12	VA2	AI	Auxiliary Analog Input
9	13	VREF	AI/AO	Voltage Reference Input/Output
10	14	VDD	DI/DO	I/O Power Supply for Data Interface
11	15	$\overline{IRQ}$	DO	Interrupt Request Signal
12	16	DOUT	DO	Data Output, Serial data is sent on the falling edge of DCLK and becomes high impedance when chip select is high.
13	1	BUSY	DO	Busy signal Output, goes to high impedance when chip select is high.
14	2	DIN	DI	Data Input. Serial data is latched on rising edge of DCLK When chip select is low.
15	3	$\overline{CS}$	DI	Chip Select Signal, high for ADC power-down.
16	4	DCLK	DI	Data Clock Input.

Table 1.Pin Description

Maximum Ratings

Characteristic	Symbol	Rating	Unit
Supply Input Voltage	VCC,VDD	-0.3 ~ +6.0	V
Analog Input Voltage		-0.3 ~ VCC+0.3	mA
Logic Input Voltage		-0.3 ~ VDD+0.3	V
Power Dissipation	PD	250	W
Maximum Junction Temperature	Tj	150	°C
Operating temperature	Top	-40~+85	°C
Storage temperature	Tstg	-65~+150	°C

Stresses beyond the Absolute Maximum ratings may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond these operational specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Maximum Ratings

Electrical Characteristics

At TA=–40°C to +85°C, +VCC=+2.7V, VREF=2.5V internal voltage, f_{SAMPLE}=125 kHz, f_{CLK}=2MHz (50% duty cycle), 12-bit mode, 0.1uF capacitor at V_{ref}, +VCC=VDD, digital inputs = VDD or GND, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DC Accuracy						
Resolution				12		Bits
No Missing Codes			10			Bits
Integral Linearity Error	INL				±3	LSB
Offset Error	OS				±6	LSB
Gain Error	GE	External VREF			±4	LSB
MOS Array						
Drive Current -		100ms - Pulse-width		50		mA
On-Resistance	Ron	YP, XP		5		Ω
		YM, XM		6		Ω
Analog Inputs						
Input Voltage range			0		VREF	V
Absolute positive input range			-0.2		+VCC+0.2	V
Absolute negative input range			-0.2		+0.2	V
Leakage Current				0.1		uA
Conversion Rate						
Conversion Time	Tcon				12	Clk Cycles
Acquisition Time	Tacq		3			Clk Cycles
Throughput Rate	Fs	16-CLKS Conversion			125	KHz
Multiplexer Settling Time				500		ns
References – Input/Output						
Internal Reference Voltage Vref			2.45	2.50	2.55	V
Internal Vref Quiescent Current				120		μA
Reference Input Range			1.0		+VCC	V
Reference Input Impedance		S/D= 0, PC1 = 0				
		Internal Reference Off		1		GΩ
		Internal Reference On		250		Ω
Battery Measurement						
Input Range			0.5		6.0	V
Input Impedance		Sampling Battery		10		KΩ
		Battery Monitor Off		1		GΩ
Accuracy		External VREF=2.5V	-2		+2	%
		Internal Reference	-3		+3	%
Temperature Measurement						
Range			-40		+85	℃
Resolution		Differential		1.6		℃
		TEMP0		0.3		℃
Accuracy		Differential		±2		℃
		TEMP0		±3		℃
Digital I/O						

Input Voltage High	Vih		VDD • 0.7		VDD + 0.3	V
Input Voltage Low	Vil		-0.3		0.3 • VDD	V
Output Voltage High	Voh	Isource=250uA	VDD • 0.8			V
Output Voltage Low	Vol	Isink=250uA			0.4	V
Power Supply						
Supply Voltage	VCC	Specified Characteristics	2.7		3.6	V
		Operating Voltage	2.2		5.25	V
IO Supply Voltage	VDD		1.5		+VCC	V
Quiescent Current		Internal Reference Off		1.75	300	µA
		Internal Reference On		295		µA
		Power Down mode with DCLK= = DIN= VDD			1	µA
Power Dissipation		+VCC = +2.7V			1.2	mW

Table 3. Electrical Specifications

Digital Timing Specifications

+Vcc=2.7 to 3.6V, Vref = 2.5V, f_{DCLKS} = 2MHz, f_{SAMPLE}=125 kHz, 12-bits mode, 0.1uF capacitors at Vref. Unless otherwise noted.

Description	Symbol	Min	Typ	Max	Units
Acquisition time	t_{ACQ}	1.5			us
DCLK Pulse Width High	t_{CH}	200			ns
DCLK Pulse Width Low	t_{CL}	200			ns
/CS Falling to First DCLK Rising	t_{CSS}	100			ns
/CS Rising to DCLK Ignored	t_{CSH}	10			ns
DIN Setup Time Prior to DCLK Rising	t_{DS}	100			ns
DIN Hold Time After DCLK High	t_{DH}	50			ns
DCLK Falling to DOUT Valid	t_{DO}			200	ns
/CS Rising to DOUT Disabled	t_{TR}			200	ns
/CS Falling to DOUT Enabled	t_{DV}			200	ns
DCLK Falling to BUSY Rising/Falling	t_{BD}			200	ns
/CS Falling to BUSY Enabled	t_{BDV}			200	ns
Rising to BUSY Disabled	t_{BTR}			200	ns

Table 4. Digital Timing Specifications

Block Diagram

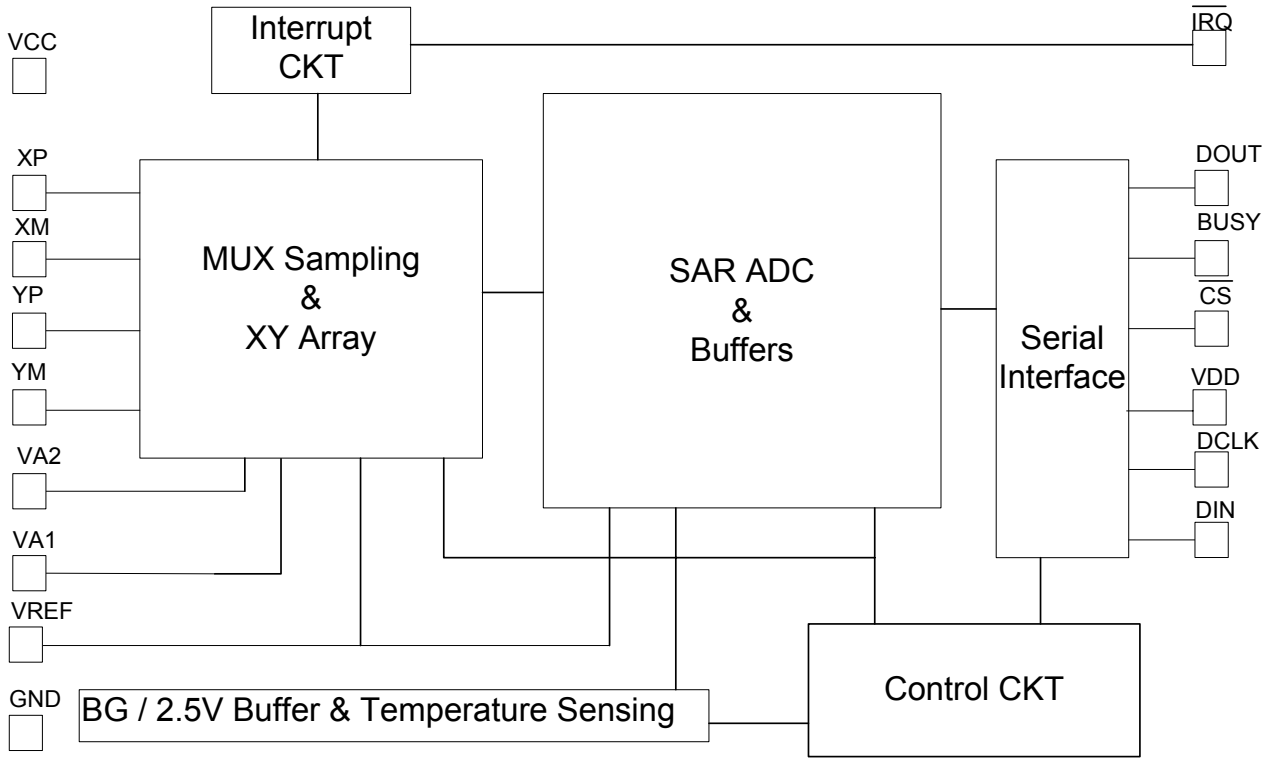


Figure 1. Functional Block Diagram

Circuit Operations

General

Figure 1 shows a functional block diagram of AUR3840 that includes a 12-bit successive approximation register (SAR) ADC, analog multiplexing, digitizing sampling and interface circuits.

The AUR3840 can be operated from a 2.2V to 5.25V power supply. The throughput rate could be 125kSPS with 2MHz clocking. The chip features an internal reference and uses an external clock. The value of the reference voltage sets the input range of the converter.

The analog input to the converter is provided via a multiplexer (MUX) that can be connected to resistive touch screen sensing signals, battery voltage, auxiliary inputs, or the chip temperature sensing voltage.

ADC Input and Conversion

The input of ADC is selected by the MUX as illustrated in Figure 2 with an address setting according to Table 5. The input control bits are provided serially via the DIN pin. An ADC operation starts after the internal sampling capacitor is fully charged from the input circuit, then the digital conversion completes with a charge transferring process via ADC's binary capacitor array. The differential voltage of +REF and -REF defines the full swing voltage of ADC input with register settings as shown in Table 6. The conversion range of AUR3840 covers 1V to Vcc.

The ADC conversions can be made in differential mode (DM) or single-ended mode (SEM) according the register setting. In single-ended mode, the +REF is connected to VREF and –REF is connected to GND. Usually the VREF was connected to VCC to obtain the maximum full swing voltage for ADC conversion.

In single-ended measurement of resistive touch screen, both gain shift and offset error may occur due to the on-resistance of the MOS array switches. There may be also tracking errors due to the resistance changes of the switches and touch screen over temperature and voltage supply. This situation can be improved in a differential mode measurement.

In the differential mode, the +REF and -REF of ADC was obtained by the sampling voltages of XP (or YP) and XN (or YN), respectively. This establishes the ADC conversion ratio metric as independent of the voltage drop across the array switches and variation of the touch screen resistance.

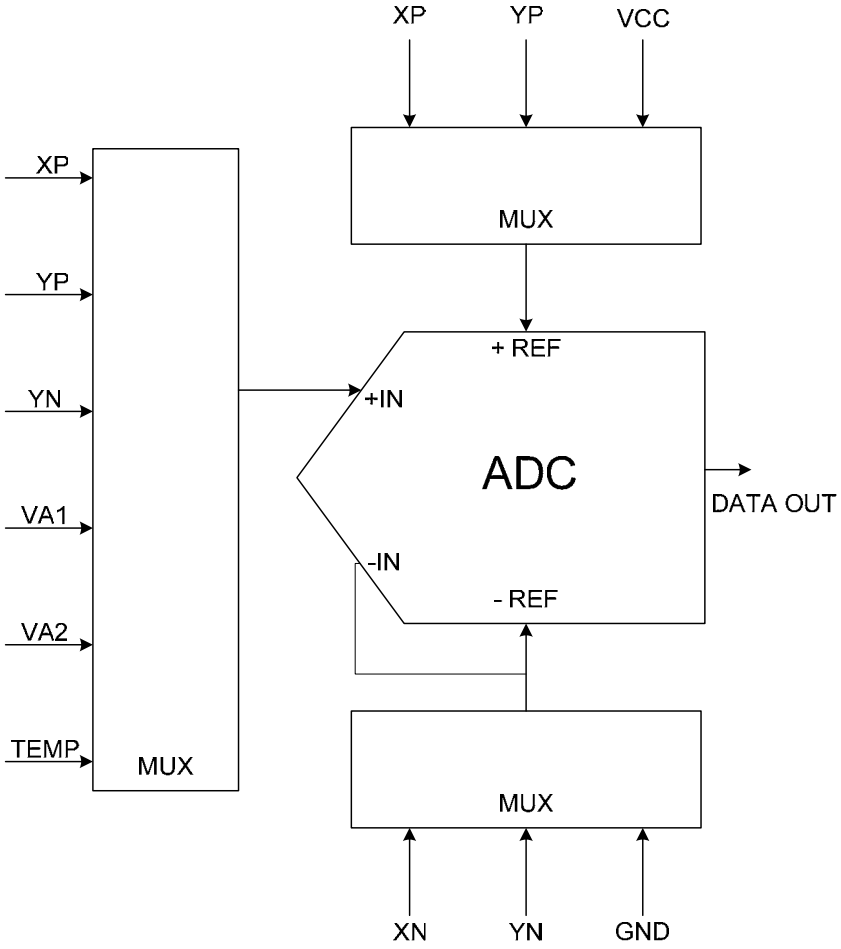


Figure 2. Analog Input Circuit Block Diagram

A2	A1	A0	S/D	ADC Input	X Switches	Y Switches	+ REF	– REF
0	0	0	1	TEMP0	OFF	OFF	VREF	GND
0	0	1	1	XP	OFF	ON	VREF	GND
0	1	0	1	VA1	OFF	OFF	VREF	GND
0	1	1	1	XP	XN ON	YP ON	VREF	GND
1	0	0	1	YN	XN ON	YP ON	VREF	GND
1	0	1	1	YP	ON	OFF	VREF	GND
1	1	0	1	VA2	OFF	OFF	VREF	GND
1	1	1	1	TEMP1	OFF	OFF	VREF	GND
0	0	1	0	XP	OFF	ON	YP	YN
0	1	1	0	XP	XN ON	YP ON	YP	XN
1	0	0	0	YN	XN ON	YP ON	YP	XN
1	0	1	0	YP	ON	OFF	XP	XN

Table 5. Input Configurations

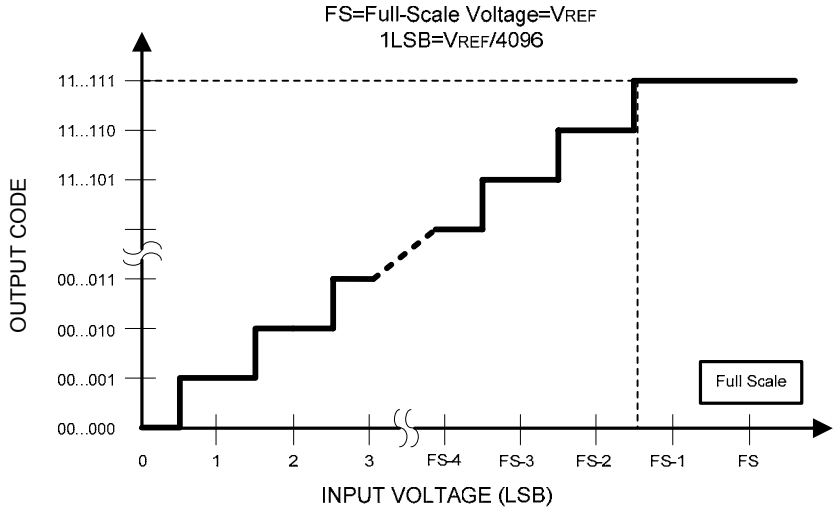


Figure 3. Ideal Input Voltages and Output Codes

Control Register

The bit assignment to the control register of the ADC is displayed in Table 6. The bits are for setting of start-conversion, channel addressing, ADC conversion resolution, reference mode and power control. The settings are described as followed: the S bit is the start bit, must be set to 1 to initiate the start of the control byte. The A2, A1 and A0 bits select the active input channel of the input multiplexer and the input switches, also decide the +REF and -REF input along with the S/D bit. The MODE bit sets the resolution of the ADC to be 12-bit or 8-bit. A setting with 0 is for 12-bit resolution and setting with 1 for 8-bit resolution. The S/D bit defines the reference mode with the settings as either differential (=low) or single-ended (=high). The PC1/PC0 bits configure the power-down mode and the interrupt function, as shown in Table 7.

BIT7	BIT 6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
S	A2	A1	A0	MODE	S/D	PC1	PC0

Table 6. Control Register Bits

PC1	PC0	$\overline{IRQ}$	DESCRIPTION
0	0	Enabled	Sets Power On/off between ADC Conversions
0	1	Disabled	Sets Reference off and ADC on
1	0	Enabled	Sets Reference on and ADC off
1	1	Disabled	Sets Reference on and ADC on

Table 7. Power Control selection

Serial Data Operation and Interface

Figure 4 shows a typical operation of the AUR3840 with digital serial interface. The serial clock provides the conversion clocking and controls the transfer of data with the AUR3840. One full conversion can be provided with 24 clock cycles of the DCLK input. When $\overline{CS}$ is high, the BUSY pin and DOUT pin are in tri-state and the AUR3840 is disabled. Once the $\overline{CS}$ signal becomes active in low, both BUSY and DOUT pins go low as well.

The control register is written via the DIN pin in the first 8 DCLK cycles. After setting of MODE bit and other associated control bits, AUR3840 starts an acquisition mode. The input signal is sampled and the BUSY pin goes high for a hold mode with three additional DCLK cycles. The touch panel switches can be turned off accordingly at this state. For next 12 DCLK cycles the ADC enters the conversion phase and outputs the conversion results from MSB to LSB for DOUT at 13th clock cycle. The total sequence takes only 21 DCLK cycles.

The 3 additional DCLK cycles were presented because of the availability of 24 DCLK cycles from a digital signal processor (DSP) or three bursts of 8 clock cycles from a microcontroller. The AUR3840 is fully powered while other serial data interfaces are operational during a conversion.

Digital Interface Timing

Figure 5 shows the detailed timing of digital interface of AUR3840. Table 4 is the corresponding timing specification.

The operation with 15 Clocks per Cycle provides the maximum conversion rate, as shown in Figure 6 timing diagram.

For 16 Clocks per Cycle conversion, the register sequence can be set with the previous conversion phase as shown on Figure 7. In this case, only two set of 8 clock cycles will be needed to complete a conversion.

For 8 Bit Conversion, the AUR3840 can operate in an 8-bit mode. Such conversion is done 4 clock cycles lesser time than a 12-bit resolution mode. The clock rate could be set higher for a 50% faster throughput rate in this mode.

Interrupt Request

The interrupt function is enabled by register PC0 as shown in Table 7. If the function is enabled, the pin goes low when the touch screen is touched. If the screen is not touched, the pin stays high.

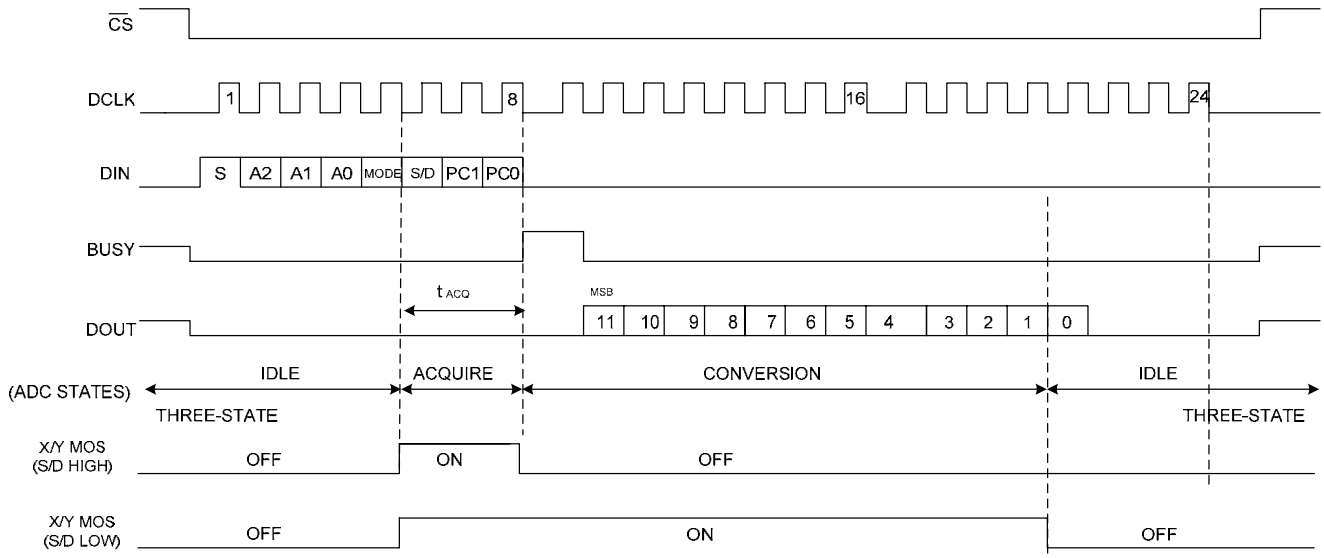


Figure 4. Conversion Timing, 24-Clock Per Conversion, 8-Bit Bus Interface

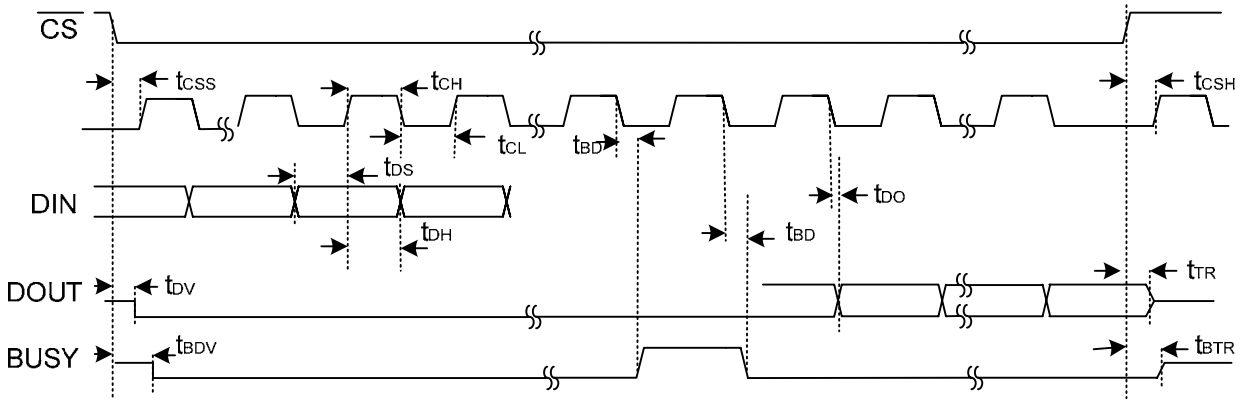


Figure 5. Digital Timing Diagram

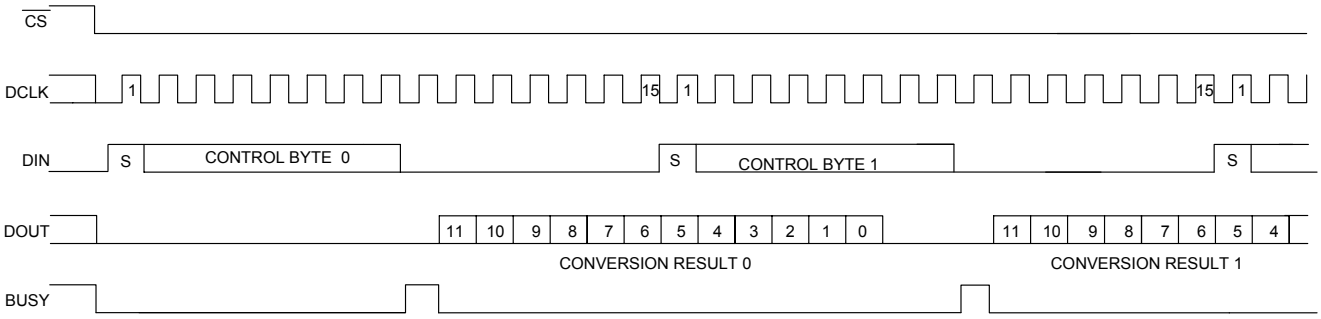


Figure 6. 15-Clock/Conversion Timing

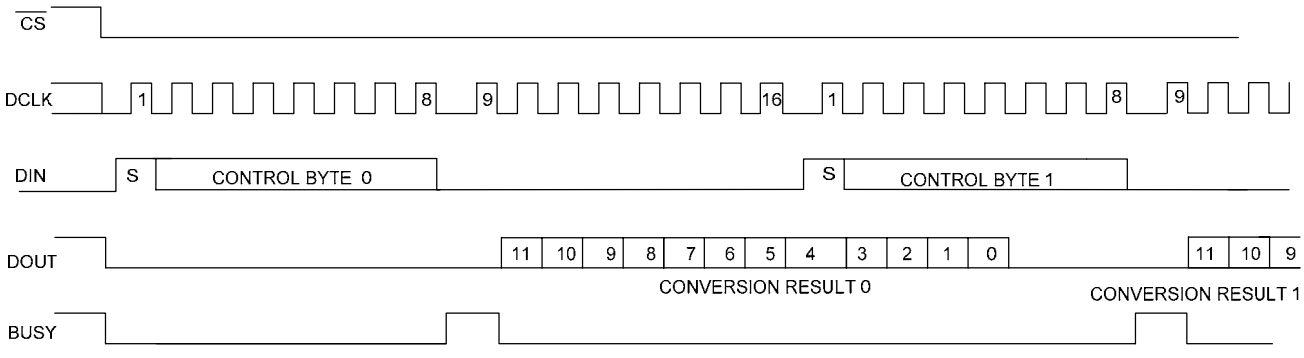


Figure 7. 16-Clock/Conversion Timing

Temperature Measurement

The temperature measurement circuit is designed according to the forward voltage (VBE) property of the internal diode that presents a known characteristic versus temperature. The circuit offers two temperature measuring modes. The first mode is the single conversion mode with the diode voltage stored at a known calibration temperature, and the ambient temperature can be estimated by the subsequent loading of the diode voltage. The second mode operates with a two-step measurement. The first step is performed with a fixed bias current into a diode, and the second step is performed with a 91 times larger bias current into the same diode. The voltage difference in the diode is proportional to absolute temperature. This second measurement mode improves the absolute temperature measurement over the first mode.

Battery Measurement

The AUR3840 can be used to monitor the battery voltage from 0V to 6V. The input voltage is divided by 4 before entering the ADC circuit. To save the power, the divider is turned on only during the sampling of the voltage.

Application Circuit

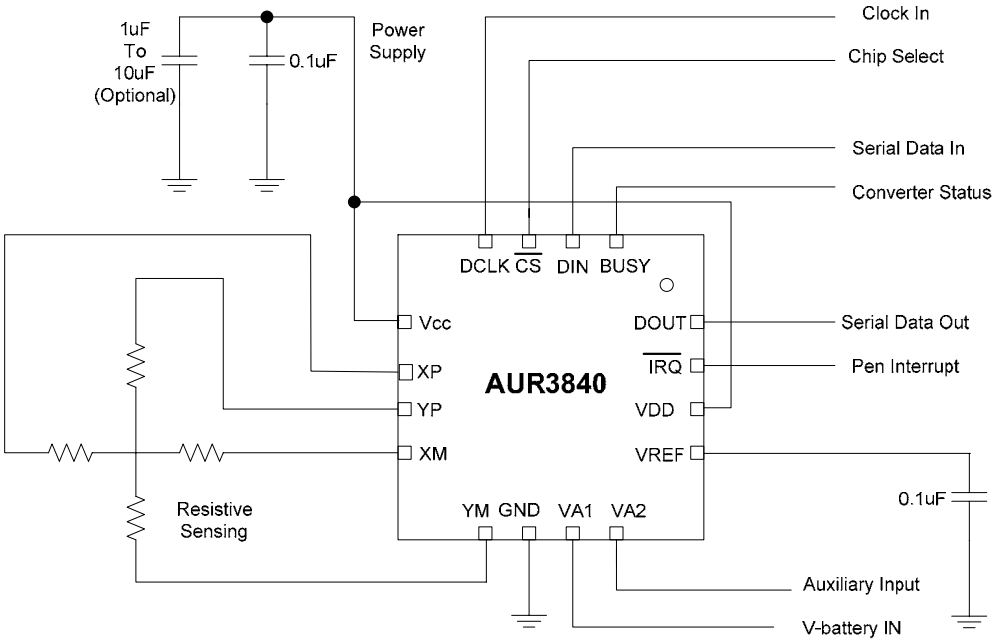


Figure 8. Typical Application Circuit

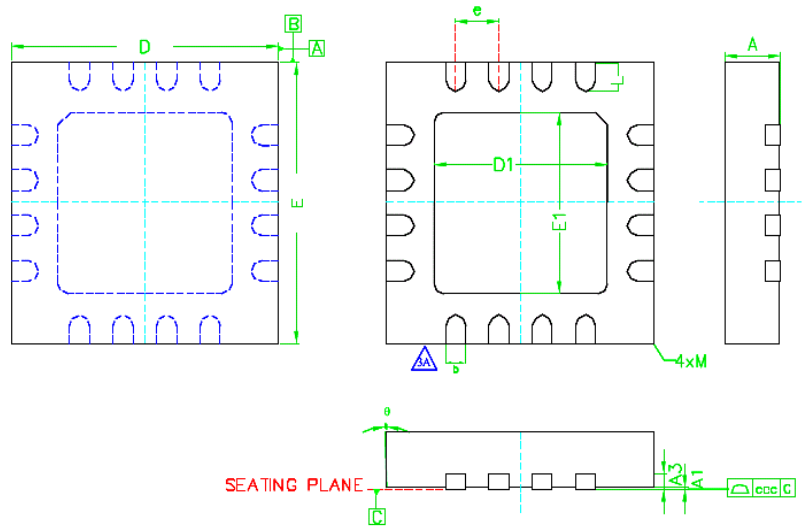
Figure 8 shows a connection diagram for AUR3840 in a resistive sensing touch screen control application.

Product Packing Specification:

Tape and Reel Information

Package Type	No of Pins	Package Size	Units Per Reel	Reel Size Reel/Hub	Trailer "A"		Leader "B"		Pocket Type	
					Pockets	Length	Pockets	Length	Width	Pitch
TSSOP	16	4.4x 5.0mm	2500	13"/4"	77	616mm	77	616mm	12mm	8mm
QFN	16	4.0x 4.0mm	2500	13"/4"	77	616mm	77	616mm	12mm	8mm

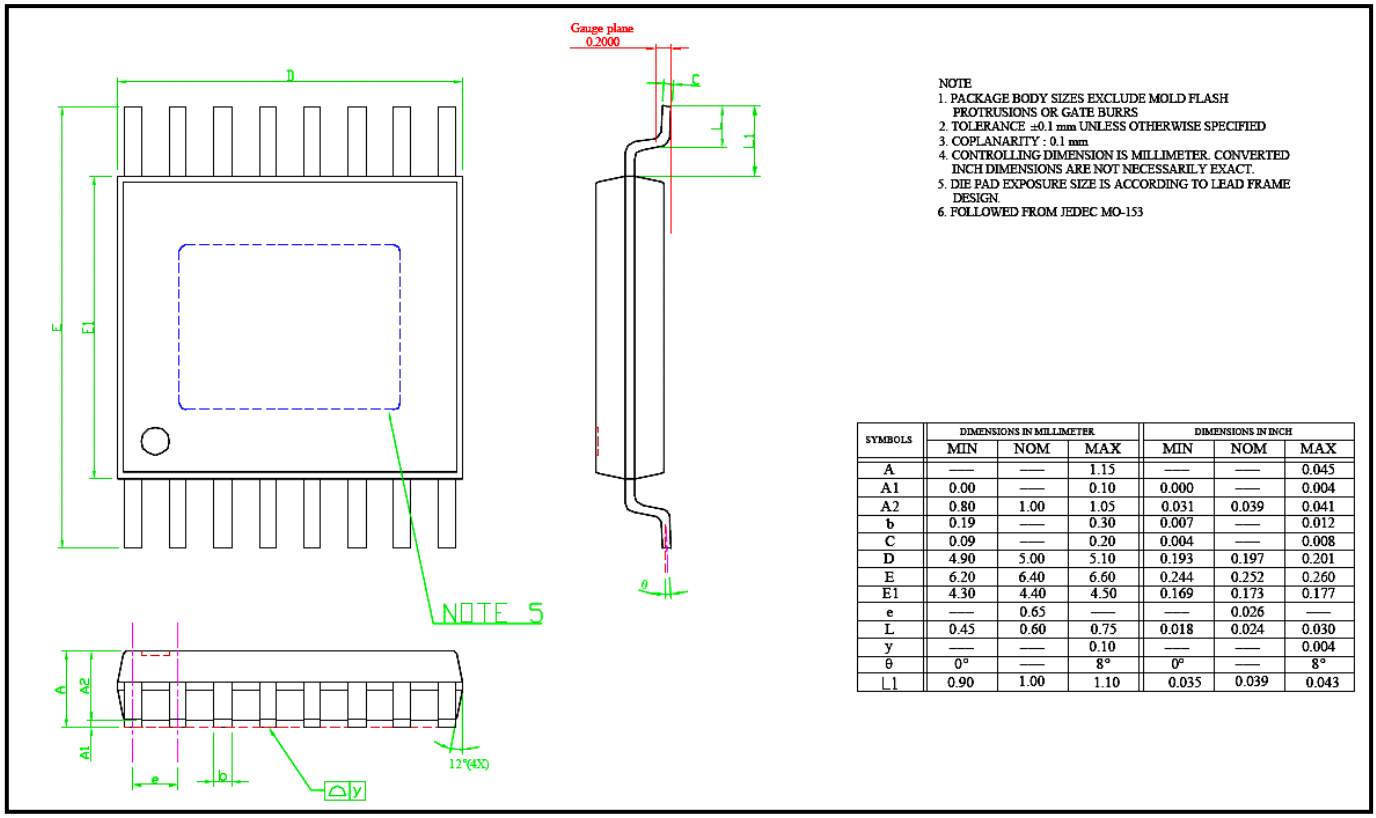
Packaging Outline Specification



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.010	0.030
A3	——	0.20REF.	——
b	0.25	0.30	0.35
D	3.95	4.00	4.03
D1	——	2.60BSC	——
E	3.95	4.00	4.03
E1	——	2.60BSC	——
e	——	0.65BSC	——
L	0.35	0.40	0.45
θ	−12	——	0
ccc	——	0.08	——
M	——	——	0.05
Burr	0	0.030	0.060

1.ALL DIMENSIONS ARE IN MILLMETERS, θIS IN DEGREES.
2.M : THE MAXIMUM ALLOWABLE CORNER ON THE MOLDED PLASTIC BODY CORNERS.
3.DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
4.DIMENSION E DOES NOT INCLUDE INTERTERMINAL MOLD PROTRUSIONS OR TERMINAL PROTRUSIONS.INTERMINAL MOLD PROTRUSIONS AND/OR TERMINAL PROTRUSIONS SHALL NOT EXCEED 0.20mm PER SIDE.
5.DIMENSION b APPLIES TO PLATED TERMINALS. DIMENSION A1 IS PRIMARILY Y TERMINAL PLATING,BUT MAY OR MAY NOT INCLUDE A SMALL PROTRUSION OF TERMINAL BELOW THE BOTTOM SURFACE OF THE PACKAGE.
6.JEDEC STANDARD MO-220

◎ AUR3840 Package Outline Specification –QFN16L



NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
2. TOLERANCE ±0.1 mm UNLESS OTHERWISE SPECIFIED
3. COPLANARITY : 0.1 mm
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. DIE PAD EXPOSURE SIZE IS ACCORDING TO LEAD FRAME DESIGN.
6. FOLLOWED FROM JEDEC MO-153

SYMBOLS	DIMENSIONS IN MILLIMETER			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	——	——	1.15	——	——	0.045
A1	0.00	——	0.10	0.000	——	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	——	0.30	0.007	——	0.012
C	0.09	——	0.20	0.004	——	0.008
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	——	0.65	——	——	0.026	——
L	0.45	0.60	0.75	0.018	0.024	0.030
y	——	——	0.10	——	——	0.004
θ	0°	——	8°	0°	——	8°
L1	0.90	1.00	1.10	0.035	0.039	0.043

◎ AUR3840 Package Outline Specification – TSSOP16L