1.5MHz, 1A, Step-Down DC-DC Converter

Features

- High efficiency Buck Power Converter
- Low Quiescent Current
- 1A Output Current
- Adjustable Output Voltage from 1V to 3.3V
- Wide Operating Voltage Ranges : 2.5 V to 5.5 V
- Built-in Power Switches for Synchronous Rectification with high Efficiency
- 600mV Feedback Voltage
- 1.5MHz Constant Frequency Operation
- Automatic PWM/LDO Mode switching control
- Thermal Shutdown protection
- Low Drop-out Operation at 100% Duty-Cycle
- No Schottky Diode Required

Applications

- Mobile Phones, Digital Cameras and MP3 Players
- Headsets, Radios and other Hand-Held Instruments
- Post DC-DC Voltage Regulation
- PDA and Notebook Computers

Description

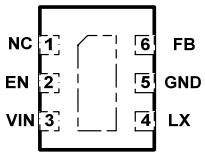
AUR9705 is a high efficiency step-down DC-DC voltage converter. The chip operation is optimized using constant frequency, peak-current mode architecture with built-in synchronous power MOS switchers and internal compensators to reduce external part counts. It is automatically switching between the normal PWM mode and LDO mode to offer improved system power efficiency covering a wide range of loading conditions.

The oscillator and timing capacitors are all built-in providing an internal switching frequency of 1.5MHz that allows the use only small surface mount inductors and capacitors for portable product implementations.

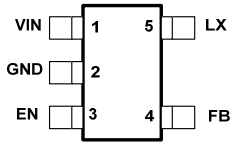
Additional features included integrated soft-start (SS), under-voltage-lock-out (UVLO) and thermal shutdown detection (TSD) to provide reliable product applications.

The device is available in adjustable output voltage versions ranging from 1v to 3.3V, and is able to deliver up to 1A.

Package Information



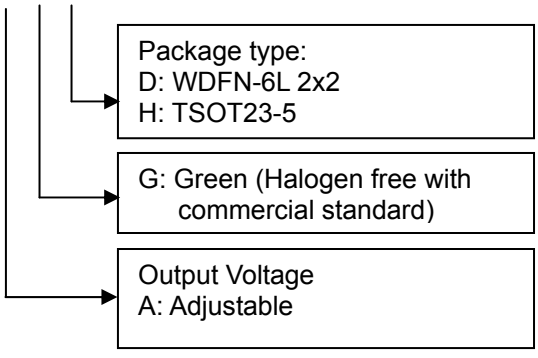
WDFN-6L 2x2



TSOT23-5

Order Information

AUR9705□□□



Typical Application Circuits

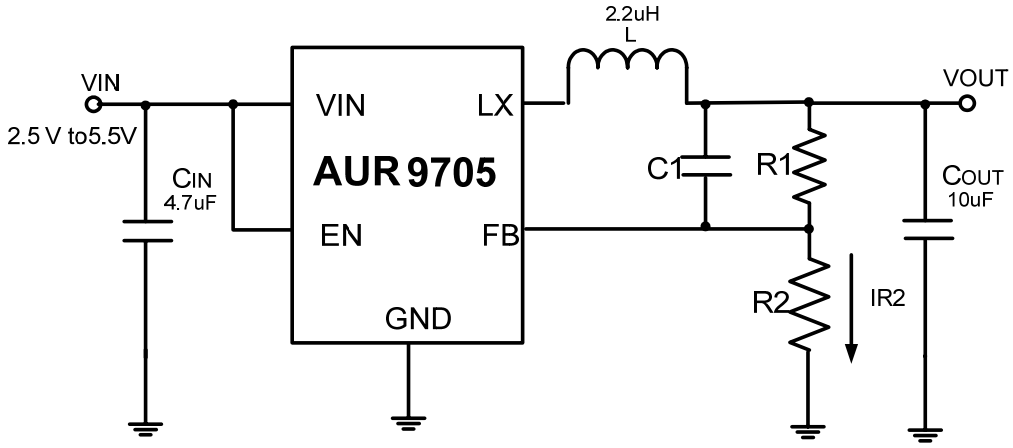


Figure 1. Adjustable Voltage Regulator

$$V_{OUT} = V_{REF} \times (1 + \frac{R_1}{R_2})$$

With R2=300 KΩ to 60 KΩ so the I_{R2}=2uA to 10uA

And (R1 x C1) should be in the range between 3×10^{-6} and 6×10^{-6} for component selection for component selection

VOUT	R1(kΩ)	R2(kΩ)	C1(pF)	L1(uH)
3.3V	240	53	20	2.2
2.5V	240	75	20	2.2
1.8V	240	120	20	2.2
1.5V	240	160	20	2.2
1.2V	240	240	20	2.2
1.0V	240	300	20	2.2

Table 1. Component guide

Pin Functions

Pin No.		Pin Name	Pin Function
TSOT23-5	WDFN-6L		
3	2	EN	Enable Signal Input, Active High.
2	5	GND	This pin is the GND reference for the NMOS power stage. It must be connected to the system ground.
5	4	LX	Connect to Inductor
1	3	VIN	Power supply input
4	6	FB	Feedback voltage from the output of the power supply.
none	1	NC	No Internal Connection (Floating or Connecting to GND)

Maximum Ratings

Characteristic	Symbol	Rating	Unit
Supply Input Voltage	V_{IN}	0~7.0	V
Enable Input voltage	V_{EN}	-0.3~VIN+0.3	V
Output Voltage	V_{OUT}	-0.3~VIN+0.3	V
Bypass Pin Voltage	V_{BP}	-0.3~VIN+0.3	V
Power Dissipation, WDFN-6L 2x2 (on PCB, Ta=30°C)		2.67	W
Thermal resistance, WDFN-6L 2x2 (simulation)	θ_{JA}	48.58	°C/W
Thermal resistance, WDFN-6L 2x2 (simulation)	θ_{JC}	62.32	°C/W
Power Dissipation, TSOT23-5 (on PCB, Ta=30°C)		--	W
Thermal resistance, TSOT23-5 (simulation)	θ_{JA}	--	°C/W
Thermal resistance, TSOT23-5 (simulation)	θ_{JC}	--	°C/W
Operating junction temperature		160	°C
Operating temperature		-40~+85	°C
Storage temperature		-55~+150	°C

Recommended Operating Condition

Characteristic	Symbol	Rating	Unit
Supply Input Voltage	V_{IN}	2.5 ~ 5.5	V
Junction Temperature Range	T_J	-40 ~ 125	°C
Ambient Temperature Range	T_A	-40 ~ 80	°C

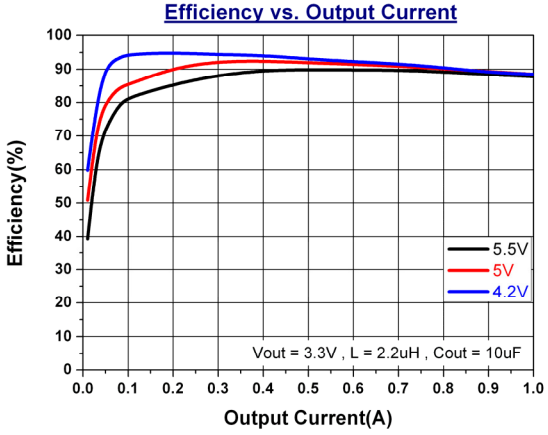
Electrical Characteristics

(Vin=3.6V, Vout=2.5V, Vref=0.6V, L=2.2uH, Cin=4.7uF, Cout=10uF, Ta=25℃, Imax=1A)

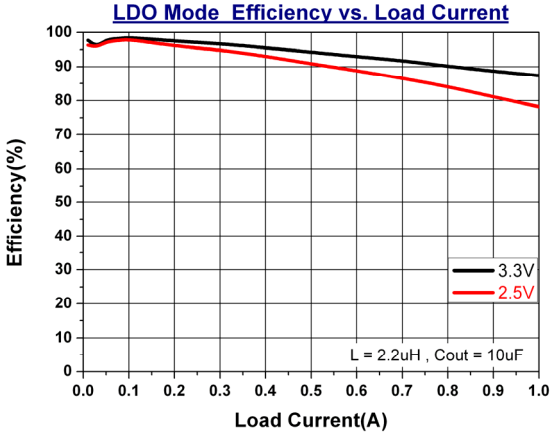
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input voltage Range	V_{IN}		2.5		5.5	V
Shutdown Current	I_{OFF}	EN=0		0.1	1	uA
Regulated Feedback voltage	V_{FB}	For adjustable output voltage	0.585	0.6	0.615	V
Regulated Output Voltage	V_{OUT}	V_{IN}=2.5V to 5.5V I_{OUT}=0mA to 1000mA	-3		+3	%
Peak Inductor Current	I_{PK}	V_{IN} =3V, $V_{FB} = 0.5V$ or V_{OUT} =90%, Duty Cycle < 35%		1.5		A
Oscillator Frequency	F_{OSC}	V_{IN} =3.6V	1.2	1.5	1.8	MHz
PMOSFET Ron	R_{ONP}	V_{IN} =3.6V, I_{OUT} =200mA		0.28		Ω
NMOSFET Ron	R_{ONN}	V_{IN} =2.5V, I_{OUT} =200mA		0.38		Ω
Input DC Bias Current	I_S	V_{IN} =3.6V, I_{OUT} =200mA		0.25		uA
		V_{IN} =2.5V, I_{OUT} =200mA		0.35		
LX leakage	I_{LX}	$V_{FB} = 0.5V$ or $V_{OUT} = 90\%$, $I_{LOAD} = 0A$		100		uA
		V_{EN}=0, V_{LX}=0V, 5V, V_{IN} =5V		0.01	0.1	
Feedback Current	I_{FB}				30	nA
En Leakage Current	I_{EN}			0.01	0.1	uA
En High-Level Input Voltage	V_{ENH}	V_{IN} =2.5V ~ 5.5V	1.5			V
En Low-Level Input Voltage	V_{ENL}	V_{IN} =2.5V ~ 5.5V			0.6	V
Under Voltage Lock Out				1.8		V
Hysteresis				0.1		V
Thermal Shutdown	T_{SD}			150		℃

Typical Performance Characteristics

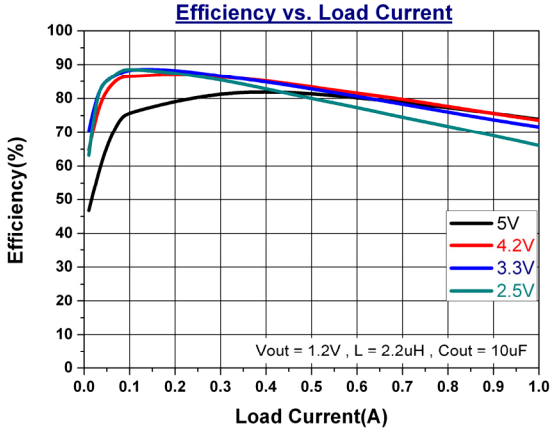
Efficiency vs. Output Current



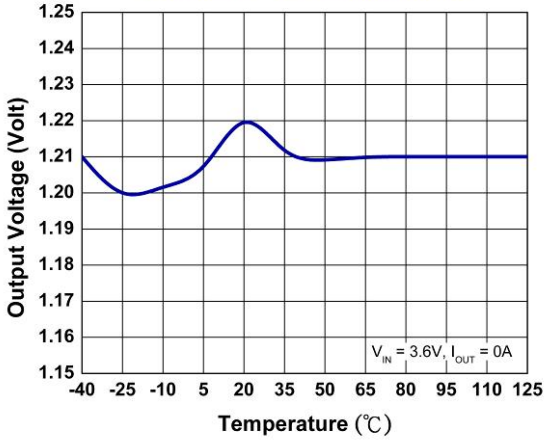
LDO Mode Efficiency vs. Load Current



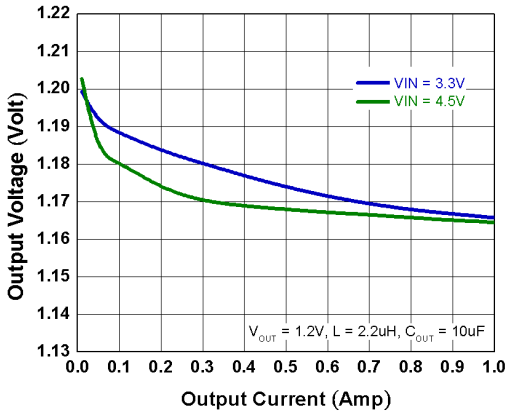
Efficiency vs. Load Current



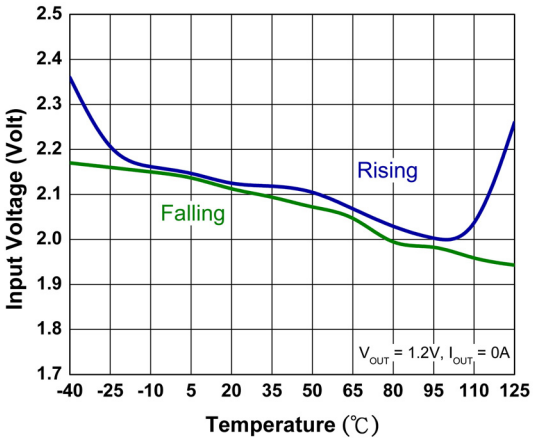
Output Voltage vs Temperature



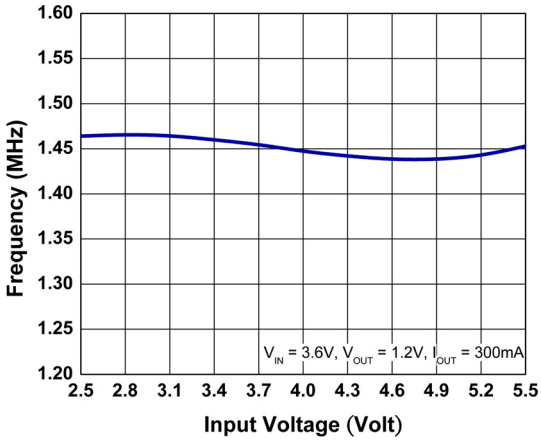
Output Voltage vs Output Current



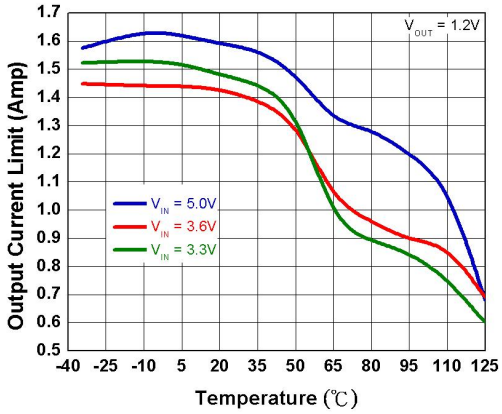
UVLO Voltage vs Temperature



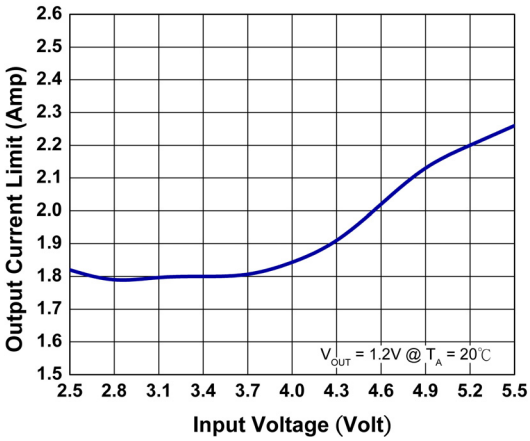
Frequency vs Input Voltage



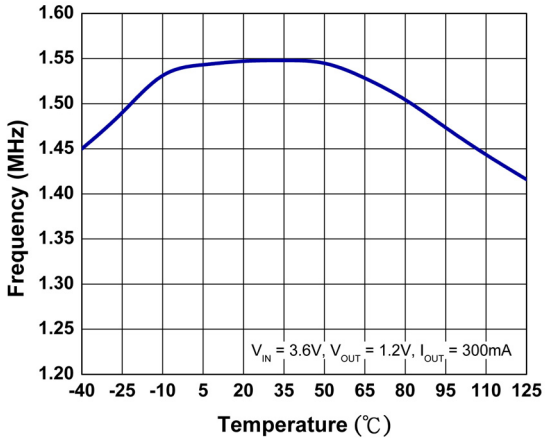
Output Current Limit vs Temperature



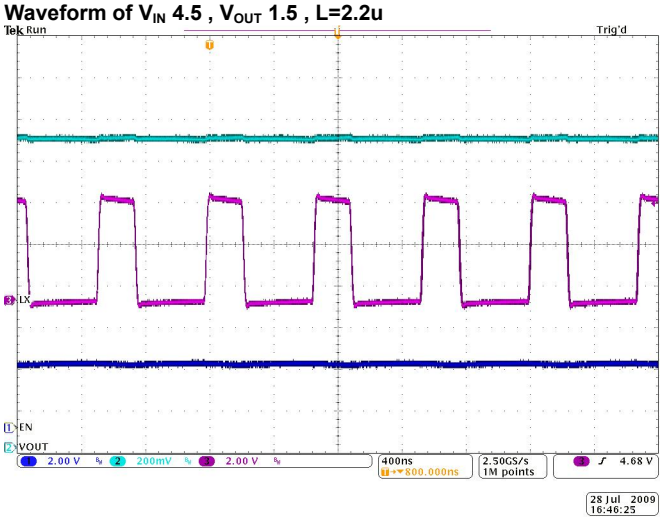
Output Current Limit vs Input Voltage



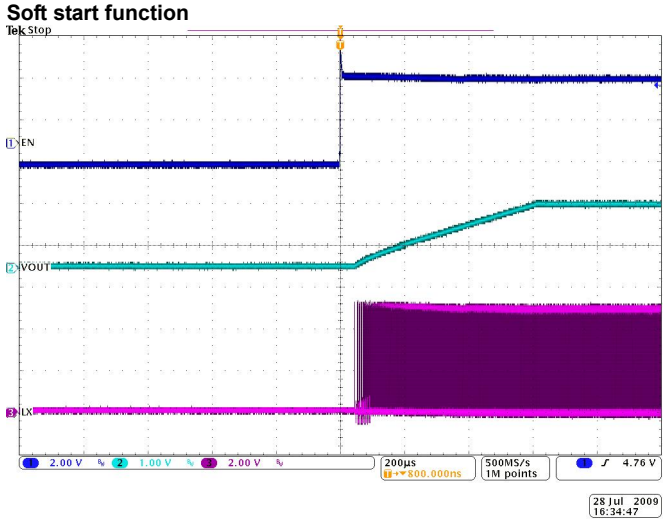
Frequency vs Temperature



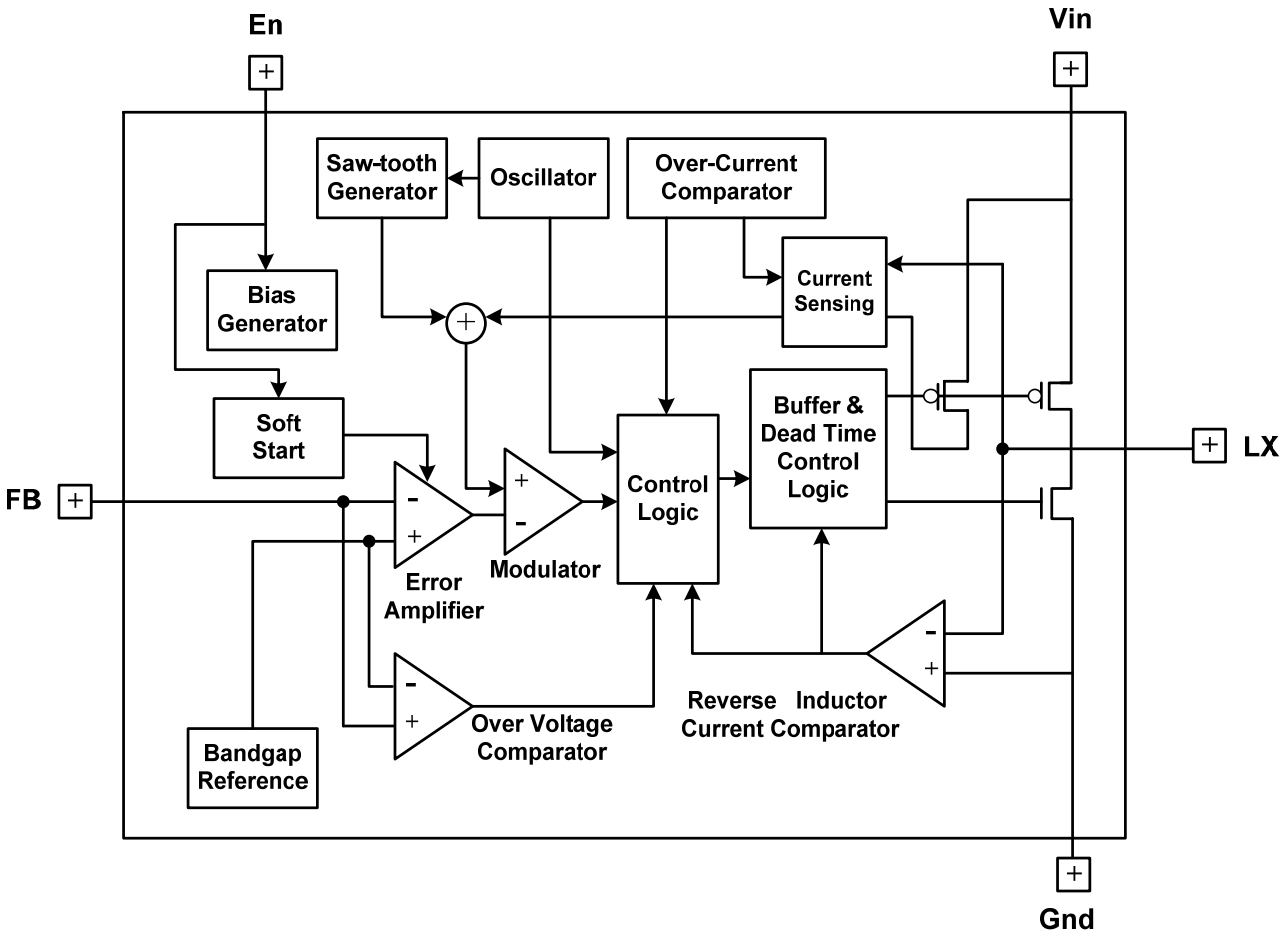
Waveform of V_{IN} 4.5 , V_{OUT} 1.5 , L=2.2u



Soft start function



Block Diagram



Application Information

The basic AUR9705 application circuits are shown as in Figure 1 External components selection is determined by the load current and is critical with the selection of inductor and capacitor values.

Inductor Selection

For most applications, the value of inductor is chosen based on the required ripple current with the range of 2.2uH to 4.7uH

$$\Delta I_L = \frac{1}{f \times L} V_{OUT}(1 - \frac{V_{OUT}}{V_{IN}})$$

The largest ripple current occurs at the highest input voltage. Having a small ripple current reduces the ESR loss in the output capacitor and improves the efficiency. The highest efficiency is realized at low operating frequency with small ripple current. However, the larger value inductors will be required. A reasonable starting point for ripple current setting is $\Delta I_L = 40\% I_{MAX}$. For a maximum ripple current stays below a specified value , the inductor should be chosen according to the following equation:

$$L = [\frac{V_{OUT}}{f \times \Delta I_L(max)}][1 - \frac{V_{OUT}}{V_{IN}(max)}]$$

The DC current rating of the inductor should be at least equal to the maximum output current plus half the highest ripple current to prevent inductor core saturation. For better efficiency, the lower DC-resistance inductor should be selected.

Capacitor Selection

The input capacitance, Cin, is needed to filer the trapezoidal current at the source of the top MOSFET. To prevent the large ripple voltage, a low ESR input capacitor sized for the maximum RMS current must be used . The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OMAX} \times \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{\frac{1}{2}}}{V_{IN}}$$

It indicates a maximum value at Vin=2Vout, where $I_{RMS} = I_{OUT}/2$. This simple worse-case condition is commonly used for design because even significant deviations do not much relief. The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize output voltage ripple and load step transients, as well as the amount of bulk capacitor that is necessary to ensure the control loop is stable. Loop stability can be also checked by viewing the load step transient response as described in a latter section. The output ripple, ΔV_{OUT} , is determined by:

$$\Delta V_{OUT} \le \Delta I_L [ESR + \frac{1}{8 \times f \times C_{OUT}}]$$

The output ripple is the highest at the maximum input voltage since ΔI_L increase with input voltage.

Load Transient

A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD} \times ESR)$, where ESR is the effective series resistance of output capacitor. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During the recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Output Voltage Setting

The output voltage of AUR9705 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} \times (1 + \frac{R_1}{R_2}) = 0.6V \times (1 + \frac{R_1}{R_2})$$

The resistive divider senses the fraction of the output voltage as shown in Figure 2.

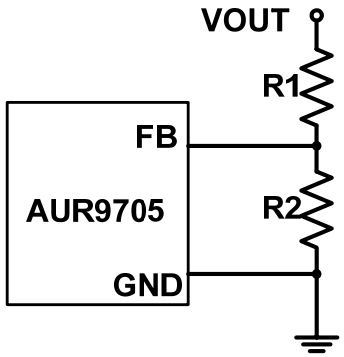


Figure 2. Setting the Output Voltage

Efficiency Considerations

The efficiency of switching regulator is equal to the output power divided by the input power times 100%. It is usually useful to analyze the individual losses to determine what is limiting efficiency and which change could produce the largest improvement. Efficiency can be expressed as:

Efficiency=100%-L1-L2-…where L1, L2,etc. are the individual losses as a percentage of input power. Although all dissipative elements in the regulator produce losses, two major sources usually account for most of the power losses: Vin quiescent current and I^2R losses. The Vin quiescent current loss dominates the efficiency loss at very light load currents but the I^2R loss dominates the efficiency loss at medium to heavy load currents.

1. The Vin quiescent current loss comprises two parts: the DC bias current as given in the electrical characteristics and the internal MOSFET switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each cycle the gate is switched from high to low to high again, the packet of charge ,dQ moves from Vin to ground. The resulting dQ/dt is the current out of Vin that is typically larger than the internal DC bias current. In continuous mode,

$$I_{gate} = f \times (Q_p + Q_n)$$

Where Q_p , Q_n are the gate charge of power PMOSFET and NMOSFET switches. Both the DC bias current and gate charge losses are proportional to the Vin and this effect will be more serious at higher input voltages.

2. I^2R losses are calculated from internal switch resistance, R_{SW} and external inductor resistance RL. In continuous mode, the average output current flowing the inductor is chopped between power PMOSFET switch and NMOSFET switch. Then, the series resistance looking into the LX pin is a function of both PMOSFET and NMOSFET Rds(on) resistance and the duty cycle (D) as follows:
   R_{SW}=[Rds(on)p * D + Rds(on)n * (1-D)
   Therefore, to obtained the I^2R losses, simply add Rsw to RL and multiply the result by the square of the average output current.

   Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2 % of total additional loss.

Thermal Characteristics

In most application, the part does not dissipate much heat due to its high efficiency. But, in some conditions where the part is operating high ambient temperature with high Rds(on) resistance and high duty cycles, such as in LDO mode, the heat dissipated may exceed the maximum junction temperature. To avoid the part from exceeding maximum junction temperature, the user should do some thermal analysis. The maximum power dissipation depends on the layout of PCB , the thermal resistance of IC package, the rate of surrounding airflow and the temperature difference between junction to ambient.

PC Board layout considerations

When laying out the printed circuit board, the following checklist should be used to optimize the performance of AUR9705.

1. The power traces, including the GND trace, the LX trace and the V_{IN} trace should be kept direct, short and wide.
2. Put the input capacitor as close as possible to the Vin and GND pins.
3. The FB pin should be connected directly to the feedback resistor divider.
4. Keep the switching node, LX, away from the sensitive FB pin and the node should be kept small area.
5. The following is an example of 2-layer PCB layout as shown in Figure 4 to Figure 5 for reference.

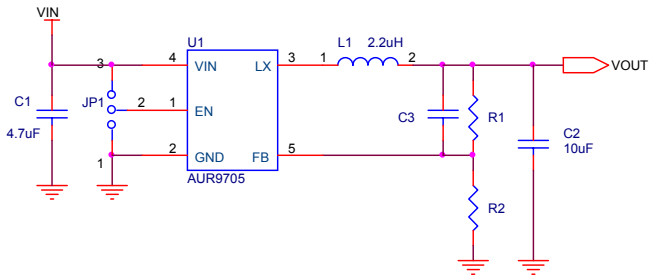


Figure 3. The Evaluation Board Schematic

Evaluation Board Layout

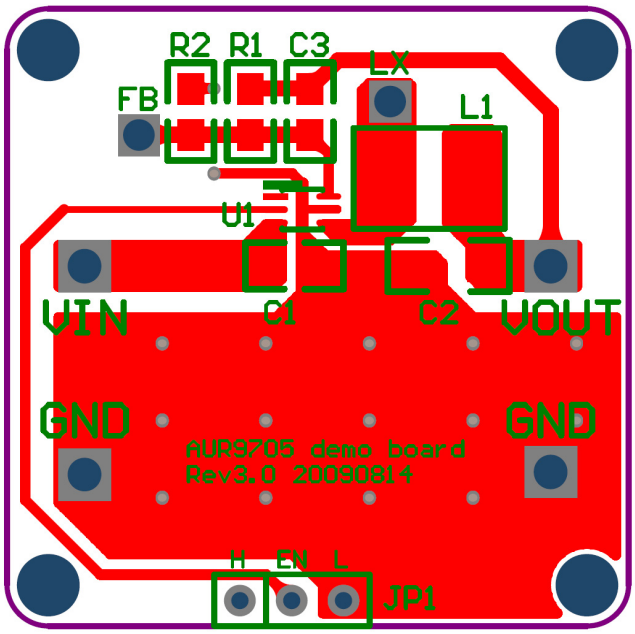


Figure 4. Top Layer Layout

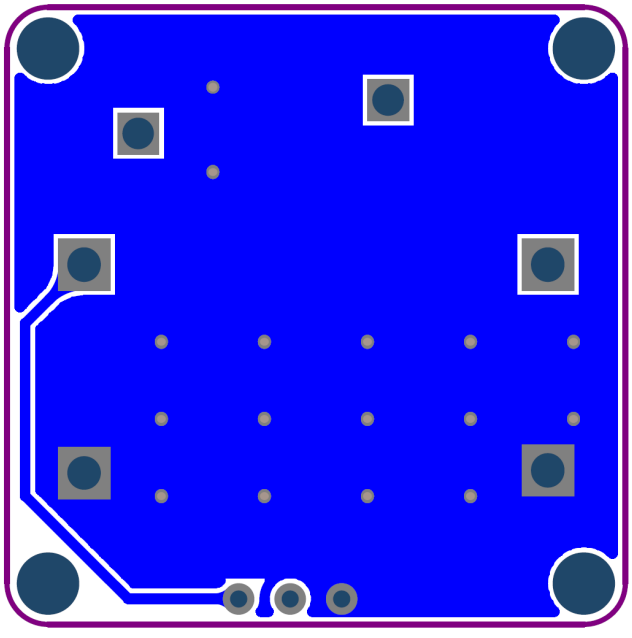
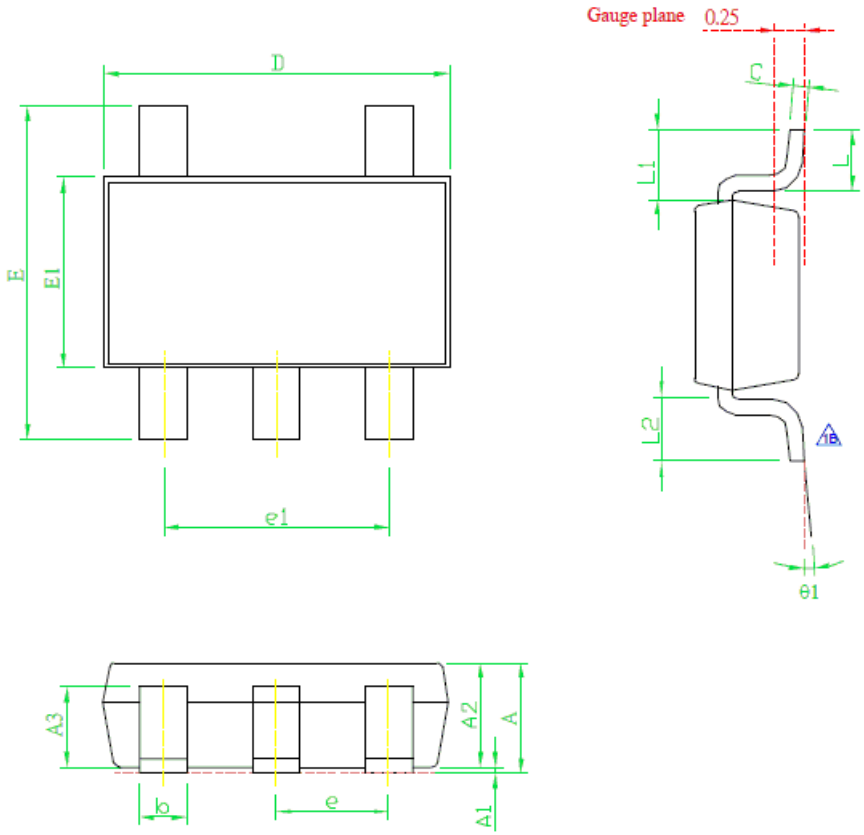


Figure 5. Bottom Layer Layout

Package Information:

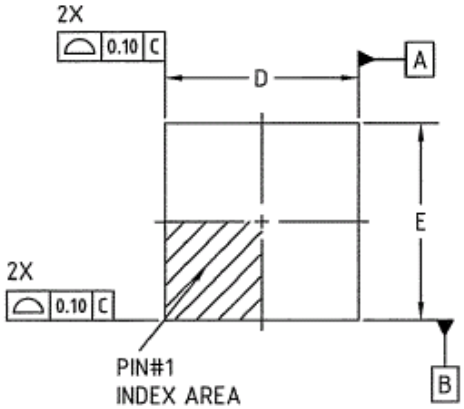
TSOT23-5

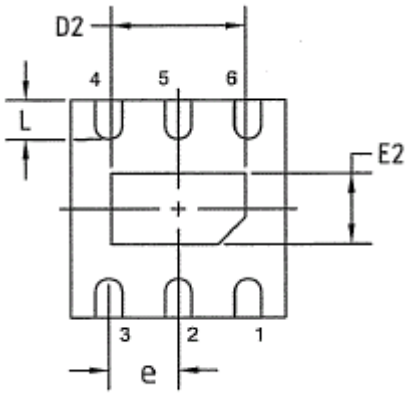


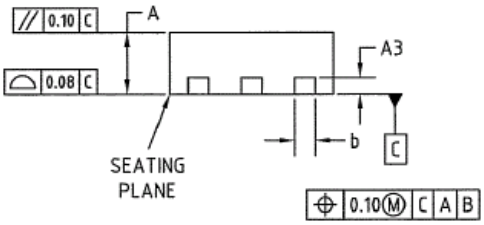
NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
2. TOLERANCE ±0.1000 mm (4 mil) UNLESS OTHERWISE SPECIFIED
3. COPLANARITY : 0.1000 mm
4. DIMENSION L IS MEASURED IN GAUGE PLANE

	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
	A	---	---	1.00
	A1	0.00	0.05	0.10
	A2	0.84	0.87	0.90
4	A3	0.58	0.68	0.78
	b	0.35	0.40	0.50
	C	0.10	0.125	0.15
	D	2.70	2.90	3.10
	E1	1.40	1.60	1.80
	e1	---	1.90(TYP)	---
	E	2.60	2.80	3.00
	e	---	0.95(TYP)	---
	θ1	1°	5°	9°
4	L	0.37	---	---
4	L1	---	0.6REF	---
4	L1-L2	---	---	0.12

WDFN-6L 2x2







SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	SEE VARIATIONS					
A3	0.20 BSC			0.008 BSC		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	2.00 BSC			0.079 BSC		
D2	1.35	1.40	1.45	0.053	0.055	0.057
E	2.00 BSC			0.079 BSC		
E2	0.55	0.60	0.65	0.022	0.024	0.026
e	0.65 BSC			0.026 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014

SYMBOL	VARIATIONS " A "					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
TDFN	0.70	0.75	0.80	0.027	0.029	0.031
DFN	0.85	0.90	0.95	0.033	0.035	0.037