Actively Alternative Mode Two-Phase / Dual Switching PWM Controller

General Description

The RT9256 is an analogous current mode design and is specifically promoted for high power density consideration platform with MLCC capacitor attached, such as high-end add-on graphic card core power and DDR SDRAM core power, etc. A highlight for RT9256 is the RichTek' s new innovation of actively alternative mode operation two-phase power conversion or dual PWM controller operation. Based on above innovation architecture, the RT9256 provides more flexibility and higher performance to customer application. The part is implemented specially for multiple power sourcing with power budget limitation. The part comes to small footprint package VQFN-32L 5x5.

Ordering Information

RT9256 □ □

- Package Type
  QV : VQFN-32L 5x5 (V-Type)
- Operating Temperature Range
  P : Pb Free with Commercial Standard

Note :

RichTek Pb-free products are :

- ▸RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▸Suitable for use in SnPb or Pb-free soldering processes.
- ▸100% matte tin (Sn) plating.

Applications

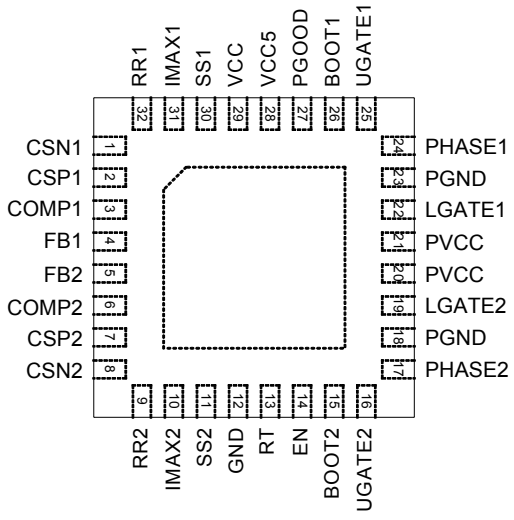
- Add-on graphic core power card
- DDR SDRAM core power
- Gaming Console
- High power density consideration platform
- Desktop/motherboard high power devices
- Power sequencing-concerned power application

Features

- **Analogous Current Mode Design**
- **Innovative Design for Actively Alternative Mode Operation :**
  - ▸**Two-Phase Power Conversion**
  - ▸**Dual PWM Controllers**
- **2.5V to 12V Switching Source Power**
- **0.8V to 3.3V Output Voltage Regulation**
- **Multiple Power Sourcing for Power Budget Limitation**
- **Adjustable V_{IN} Feed-Forward Ramp Slope**
- **Adjustable Operation Frequency**
- **Precision Core Voltage Regulation**
- **Precision DCR Current Sensing (with High Quality Capacitor, X7R)**
- **±1% V_{REF} Accuracy**
- **Input Voltage : 12V or 5V Bias**
- **Enable and PGOOD Function for Sequencing-Concerned Power**
- **Over Current Protection**
- **Over Voltage Protection**
- **External Soft Start Setting**
- **Operation Frequency Up to 1.0MHz Per Channel**
- **32-Lead VQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Pin Configurations

(TOP VIEW)



VQFN-32L 5x5

Typical Application Circuit

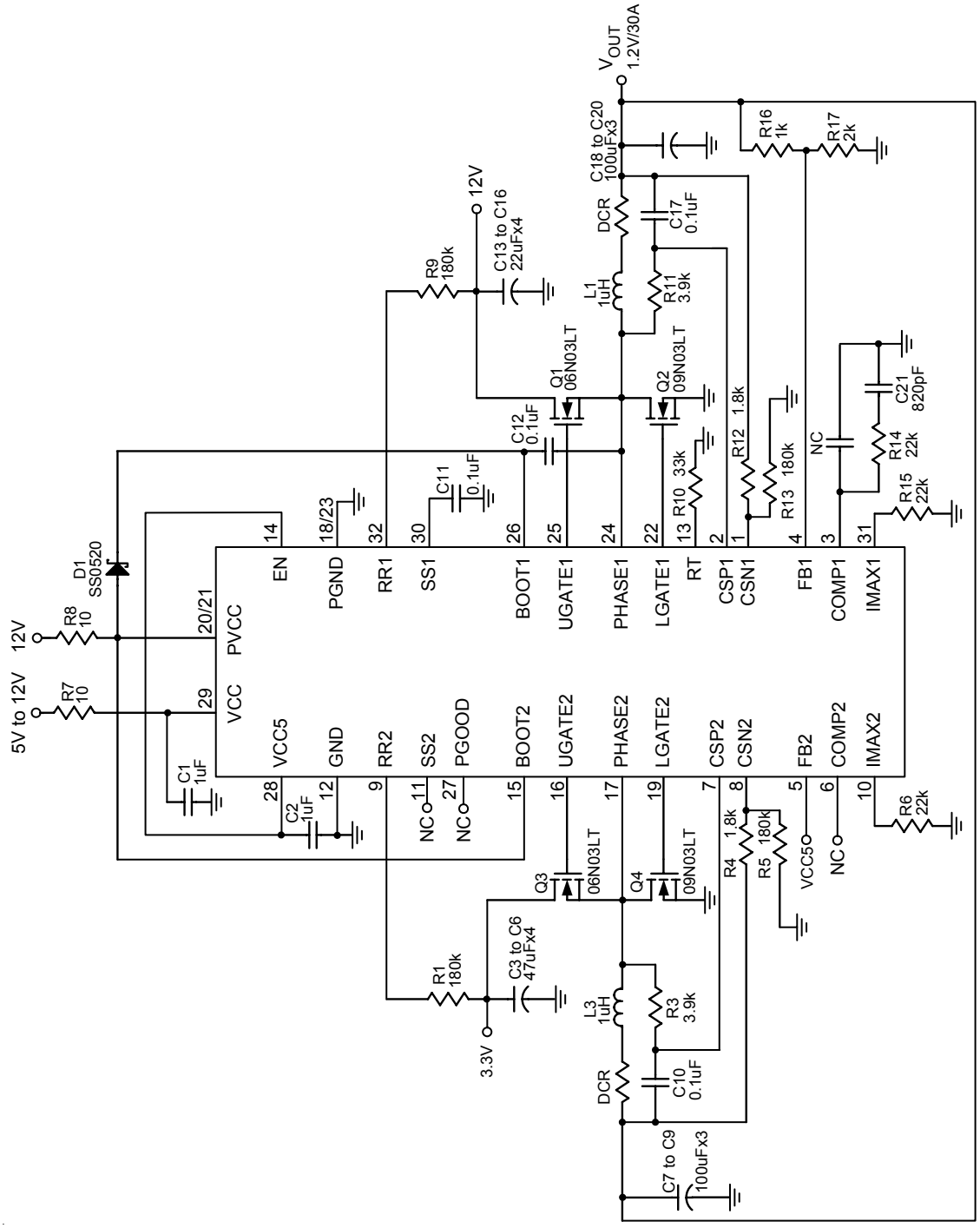


Figure 1. Two-Phase Application

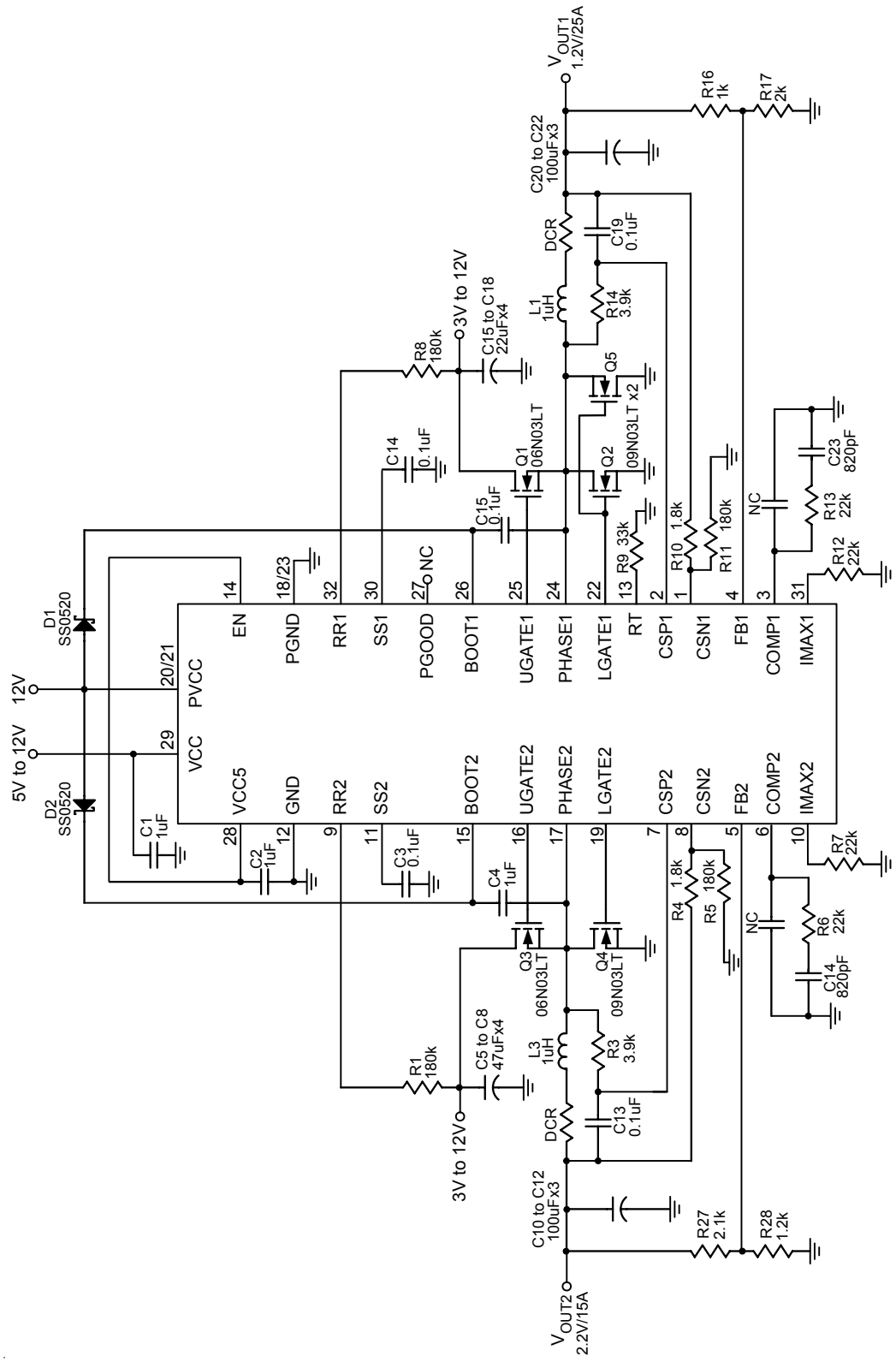
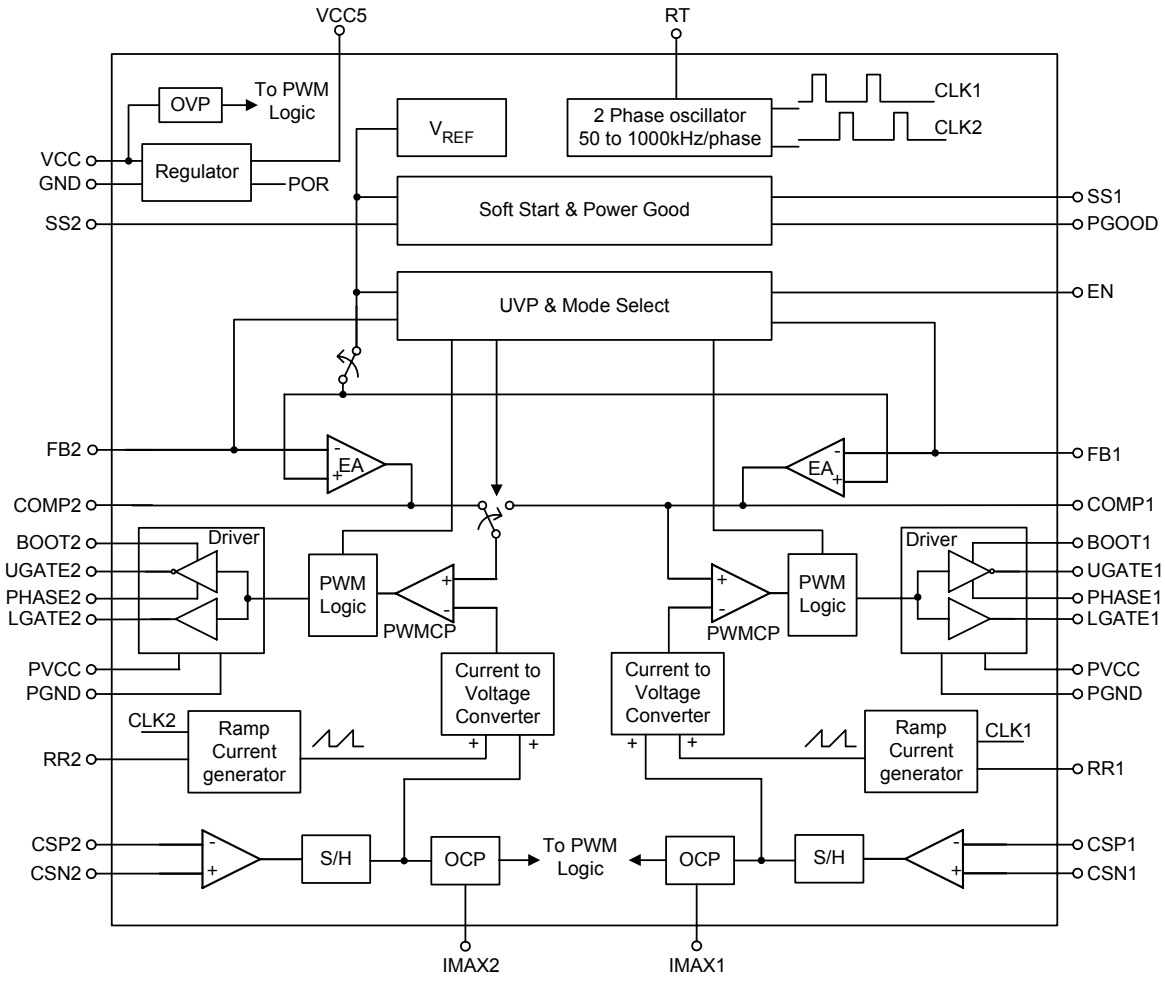


Figure 2. Two-Switcher Application

Function Block Diagram



Operation

RT9256 is a highly flexible, high performance and high precision synchronous buck controller specifically designed for high-end graphic core power supply as well as DDR applications, with highly reduced external components and costs.

RT9256 features two controllers that can be configured as a two-phase buck converter suitable for high power density applications like core power for GPU. It can also be configured as two independent buck converters for DDR power sets.

RT9256 uses RichTek proprietary Analogous Current Mode™ topology which mimics the traditional peak current mode by sensing the valley current of the inductor via DCR sensing techniques and simulating the current ramp with an artificial ramp set externally. The Analogous Current Mode topology benefits all the advantages of peak current mode converter with much higher noise immunity than conventional one. Since the compensation is easier and with less constraint than that in voltage mode, using low ESR output capacitor as MLCC is possible, which therefore dramatically reduce the board size as well as the cost and has better transient response due to higher control bandwidth. RT9256 also adopts VIN feedfoward for ramp setting, which decreases the complexity for compensation by keeping the modulator gain constant along line variations.

With the nature of current mode converter, current balance is automatically achieved in two-phase mode. By properly setting current sense resistors, current ratio other than 1 between two channels is also possible. RT9256 can also be used to form a single output voltage buck converter with dual input voltages.

Out-of-phase switching in both two-phase and two-switcher modes reduces the input current ripple and therefore reduces the component requirement as well as cost.

The wide input voltage range of the converter ranges from 3.3V to 12V. The output voltage can be set from 0.8V to 3.3V with external resistor divider. The bias voltage of the chip is VCC5.

The IC integrates two control circuits for two synchronous buck converters. The default mode of RT9256 is two switcher mode. The two phase mode can be activated by pulling FB2 pin high before POR as shown in Figure 3.

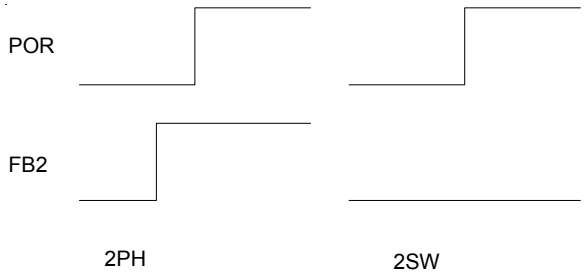


Figure 3

The power sequence of RT9256 includes: 1: POR function 2: V_{IN} power supply detection 3: EN pin setting to enable the whole chip. 4: PG to indicate the power good condition of the chip The chip will detect the voltage at FB pin when SS pass Vcc5 – 1.3 and send a PG high signal if FB > 0.6V. The power sequence of the chip is shown in Figure 4.

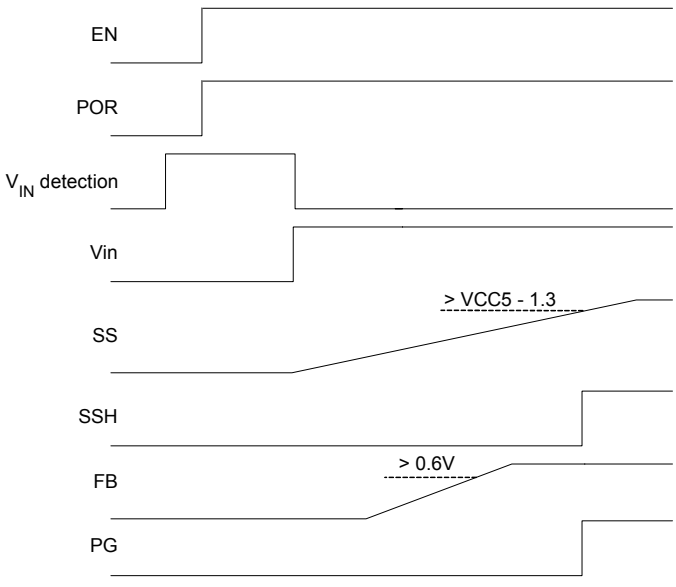


Figure 4

The external elements selection of RT9256 includes 1: RT pin resister to GND to set the operation frequency of the chip. 2: CSN pin resister to set the current gain(ratio of inductance current IL and sensed current Ix) and current scaling in two phase mode operation. 3: RR pin resister to Vin to set the slope of the Vin feed forward ramp and the effective slope compensation of current mode. 4. IMAX pin resister to GND to set the over current level 5: capacitor at SS pin to set the soft-start time 6. type two compensation at COMP pin.

Power on reset

The POR circuitry monitors the supply voltage of the chip. When the chip power supply exceeds 4.2V, the chip releases the reset state and works according to the settings. Once the supply voltage is lower than 4.0V, POR circuitry resets the chip.

V_{IN} detection

The V_{IN} detection circuitry monitors the switching power source when power up. As V_{IN} > 1.8V, RR pin is enable for ramp setting and the chip is in ramp setting mode. The voltage at RR pin will be about 0.55V. Otherwise, the chip will be in V_{IN} detection mode and RR pin is disable for ramp setting until V_{IN} > 1.8V. In V_{IN} detection mode, the UGATE and LGATE will be off and SS will be pulled low by a constant current of 10uA. The chip will enter the ramp setting mode and SS will re-softstart when V_{IN} > 1.8V.

In two switcher mode, the detection function work independently. In two phase mode, ramp setting mode will be activated when both channel' s V_{IN} are ready.

Enable

After POR reset, the chip monitors the voltage of EN pin. When V_{EN} is higher than 0.8V, the chip is enabled. The chip is disabled when V_{EN} is lower than 0.8V. With a precision threshold voltage, the EN pin can be used for power sequence.

Modes of operation

The default mode of RT9256 is two-switcher mode. Two buck controllers consisting of independent error amplifiers, PWM modulators, current sense amplifiers and ramp generators operate independently. The two-phase mode is activated by pulling FB2 high when POR. In two-phase mode, error amplifier of channel 1 performs the compensator of the converter for both channels. SS2 and COMP2 are also disabled in this mode.

Soft-start

A constant current of 10uA starts to charge the capacitor connected to SS pins right after the chip has been powered up and enabled. The ramp voltage on SS pins is also used to clamp the comp voltage during soft-start, which automatically constraints the output current due to the nature of current mode topology. This brings up smaller inrush current and smooth output voltage ramp. When the voltages on SS pins exceed VCC5-1.3V, the controller starts to monitor the voltage on FB pins. Once V_{FB} is higher than 0.6V, the open drain PGOOD pin will be turned off, i.e. released indicating power good. The SS pins are also used as the timer during OCP and UVP hiccup.

Frequency setting

The converter switching frequency is programmed by connecting a resistor from the RT pin to GND. The frequency vs. R plot is shown in "Typical Operating Characteristics".

Output voltage setting and control

In two-switcher mode, both control loops consist of an independent error amplifier, a pulse width modulator, current feed back components, a gate driver and power components. The internal high accuracy bias provides the reference voltage of 0.8V at the non-inverting input of both error amplifiers. The output voltage is programmed by using a voltage divider at output and feeding the voltage division back to corresponding error amplifiers. As conventional current mode PWM controller, the output voltage is locked at the V_{REF} of error amplifier and the error signal is used as the control signal of pulse width modulator. The PWM signals are generated by comparison of EA output and current ramp waves. Power stage transforms VIN to output by PWM signal on-time ratio.

In two-phase mode, the single output control loop consists of one error amplifier shared with two pulse width modulators, two sets of current feed back components, two gate drivers and power components. The error amplifier at channel one with pins COMP1 and FB1 is used to control the pulse width modulator. The PWM signals of each channel are generated by comparison of the error amplifier output and the independent split-channel current ramp signals.

Functional Pin Description

CSN1 (Pin 1), CSN2 (Pin 8)

Current Sense Negative Input. These pins are negative input nodes of the current sense amplifiers used for DCR current sensing. Connect this pin with a resistor to the output node.

CSP1 (Pin 2), CSP2 (Pin 7)

Current Sense Positive Input. These pins are positive input nodes of the current sense amplifiers used for DCR current sensing. Connect this pin to the junction of the filter resistor and capacitor.

COMP1 (Pin 3), COMP2 (Pin 6)

Compensation Pin. In dual switching mode, these pins are output nodes of the error amplifiers. In two phase mode, only COMP1 is active.

FB1 (Pin 4), FB2 (Pin 5)

Feedback Pin. In dual-switching mode, these pins are negative input pins of the error amplifiers.When SS pass V_{CC5} – 1.3 and FB1 or FB2 < 0.6V, the UV protection function will be activated. The two-phase mode is activated by pulling FB2 above 4V when POR. The UV protection function will be enabled if FB1 < 0.6 when the SS pass V_{CC5} – 1.3.

RR2 (Pin 9), RR1 (Pin 32)

Ramp resistor. These pins are used to set the ramp voltages. Connecting a resistor from this pin to its converter input power sets the ramping slope of the control loop of the converter. Since it is connected to converter input power, the ramp slope is input-feed-forwarded. As VIN > 1.8V, RR pin is enable for ramp setting.

IMAX2 (Pin 10), IMAX1 (Pin 31)

Maximum Current Setting. These pins set the current limiting levels. Connect these pins with resistors to ground to set the current limit.

SS2 (Pin 11), SS1 (Pin 30)

Soft-start Pin. These pins provide soft-start function for their respective controllers. The COMP voltage of the converter follows the ramping voltage on the SS pin.

RT (Pin 13)

Timing Resistor. Connect a resistor from RT to GND to set the clock frequency.

EN (Pin 14)

Enable Pin. Pull the EN pin above 0.8V at POR (VCC5 > 4.2V), the whole chip function will be enabled.

BOOT2 (Pin 15), BOOT1 (Pin 26)

Bootstrap Power Pin. These pins power the high-side MOSFET drivers. Connect this pin to the junction of the bootstrap capacitor with the cathode of the bootstrap diode. Connect the anode of the bootstrap diode to the PVCC pin.

UGATE2 (Pin 16), UGATE1 (Pin 25)

Upper Gate Drive. These pins drive the gates of the high-side MOSFETs.

LGATE2 (Pin 19), LGATE1 (Pin 22)

Lower Gate Drive. These pins drive the gates of the low-side MOSFETs.

PHASE2 (Pin 17), PHASE1 (Pin 24)

These pins are return nodes of the high-side drivers. Connect these pins to high-side MOSFET sources together with the low-side MOSFET drains and the inductor.

GND (Pin 12)

Chip Ground.

PGND (Pin 18 and 23)

Driver Ground.

PVCC (Pin 20 and 21)

Driver Power.

VCC5 (Pin 28), VCC (Pin 29)

The VCC5 pin is the internal 5.2V regulator output powered from the external voltage (VCC). VCC5 is dedicated for RT9256 internal use only and not for external power source.

PGOOD (Pin 27)

Power Good. In two-switcher mode, PGOOD is an open drain output used to indicate the status of the voltages on all SS pins, FB pins and VIN (by detecting RR at POR).

PGOOD pulled low when

1. SS1 or SS2 < V_{CC5} – 1.3

2. FB1 or FB2 < 0.6V

In two-phase mode (FB2 pulled high), PGOOD is an open drain output used to indicate the status of the voltages on SS1 pin and FB1 pin.

PGOOD pulled low when

1. SS1 < V_{CC5} – 1.3

2. FB1 < 0.6V

Absolute Maximum Ratings (Note 1)

- Supply Voltage ---------- –0.3V to 16V
- Storage Temperature Range ---------- –65°C to 150°C
- PHASE to GND
  DC ---------- –5V to 15V
  < 200ns ---------- –10V to 30V
- BOOT to PHASE ---------- 15V
- BOOT to GND
  DC ---------- –0.3V to V_{CC}+15V
  < 200ns ---------- –0.3V to 42V
- Input, Output or I/O Voltage ---------- GND–0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-32L 5x5 ---------- 1.923W
- Package Thermal Resistance (Note 4)
  VQFN-32L 5x5, θ_{JA} ---------- 52°C/W
- Operation Junction Temperature Range ---------- –40°C to 125°C
- Junction Temperature ---------- 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 1.5kV
  MM (Machine Mode) ---------- 150V

Recommended Operating Conditions (Note 3)

- Supply Input Voltage ---------- 5V to 14V
- Junction Temperature Range ---------- –20°C to 70°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, Unless Otherwise specification)

Parameter		Symbol	Test Condition	Min	Typ	Max	Units
Supply Input							
Supply Voltage		V_{CC}		4.5	12	14	V
Power On Reset		V_{CC5V}		4.0	4.2	4.4	V
Power On Reset Hysteresis				0.1	0.3	0.5	V
Enable	On	V_{EN}		0.75	0.8	0.85	V
Threshold	Hysteresis	V_{EN}		20	50	100	mV
Supply Current		I_{CC}	V_{CC} =12V, V_{SS}= 0V	3	5	10	mA
Soft Start							
Soft Start Current		I_{SS}		8	10	15	uA
Oscillator							
Frequency	Frequency	F_{OSC}	RT=33kΩ	270	300	330	kHz
	Variation		RT= 5k to 50kΩ	-10	--	10	%
Frequency Range			Per phase	50	300	1000	kHz
Maximum Duty Cycle			Per phase	70	75	80	%
Up-ramp setting pin		V_{RR}	RR = 120kΩ	0.3	0.5	0.7	V

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Reference Voltage						
Feedback Voltage	V_{FB}		0.792	0.8	0.808	V
Error Amplifier						
DC Gain			70	88	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	6	10	--	MHz
Trans-conductance	GM	R_{LOAD} = 20kΩ	630	660	--	uA/V
Maximum Output Current (source & sink)	$I_{COMP(MAX)}$	V_{COMP}=1/2 x V_{CC5}	300	360	--	uA
Current Sense GM						
Maximum Output Current (source)	$I_{GM(MAX)}$	Rsense = 2kΩ	90	--	--	uA
Gate Driver						
Maximum Upper Driver Source	I_{UGATE}	BOOT-PHASE = 12V	--	1.3	--	A
Upper Driver Sink	R_{UGATE}	V_{UGATE} = 1V	--	3	6	Ω
Maximum Lower Driver Source	I_{LGATE}	PV_{CC}=12V	--	1.5	--	A
Lower Driver Sink	R_{LGATE}	V_{LGATE} = 1V	--	1.5	3	Ω
Protection						
IMAX Voltage	V_{IMAX}	R_{IMAX} = 15kΩ	0.95	1.0	1.05	V
Under Voltage Protection	V_{FB}		0.55	0.60	0.65	V
Power Sequence						
Power Good Threshold	V_{SS}	V_{SS} pin rising	V_{CC5}–1.6	V_{CC5}–1.3	V_{CC5}–1	V
Power Good Sink Capability		I_{PGOOD} = 4mA	--	0.05	0.2	V

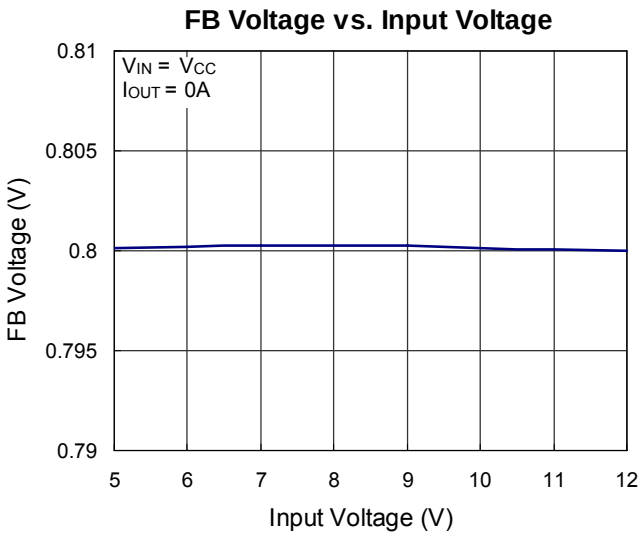
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

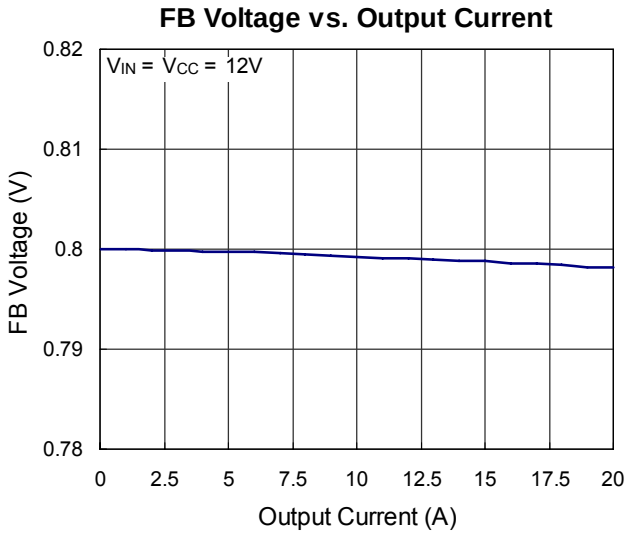
Note 2. Devices are ESD sensitive. Handling precaution recommended.

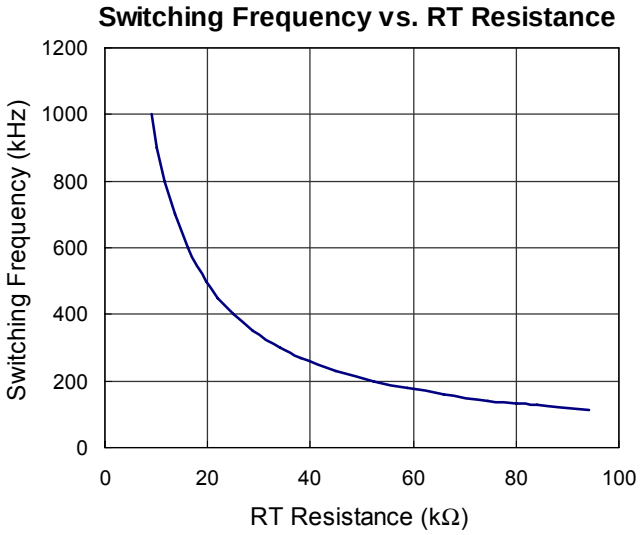
Note 3. The device is not guaranteed to function outside its operating conditions.

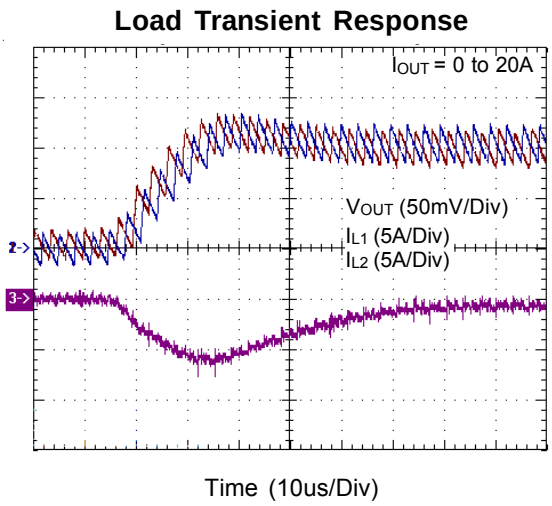
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

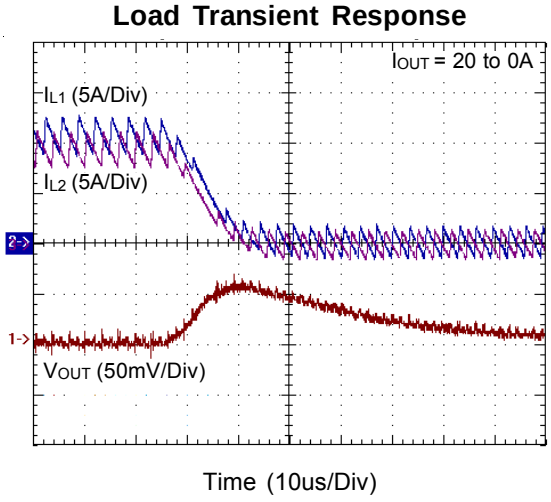
Typical Operating Characteristics

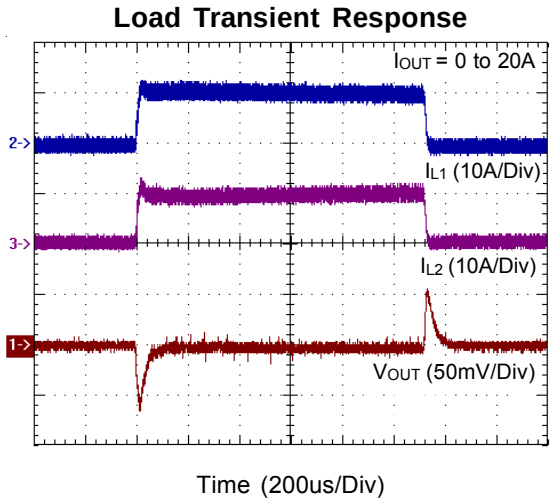




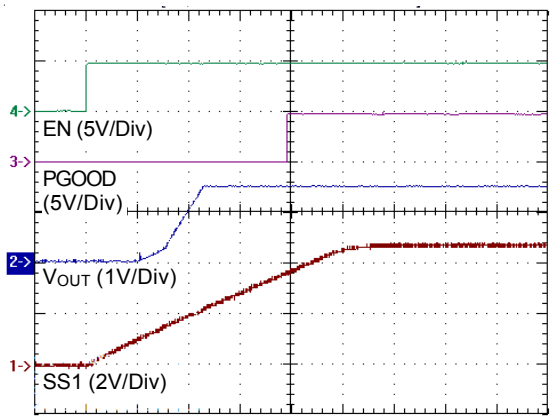






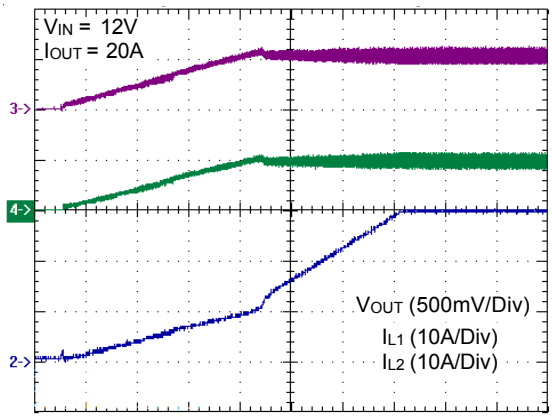


Turn On



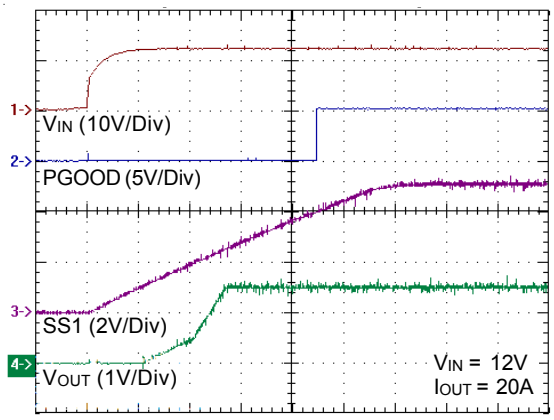
Time (10ms/Div)

Power Up



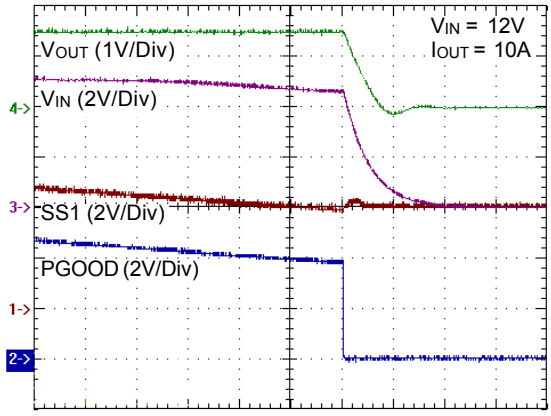
Time (2ms/Div)

Power Up



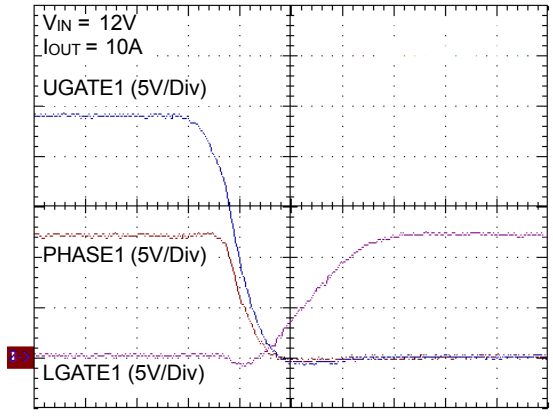
Time (10ms/Div)

Power Off



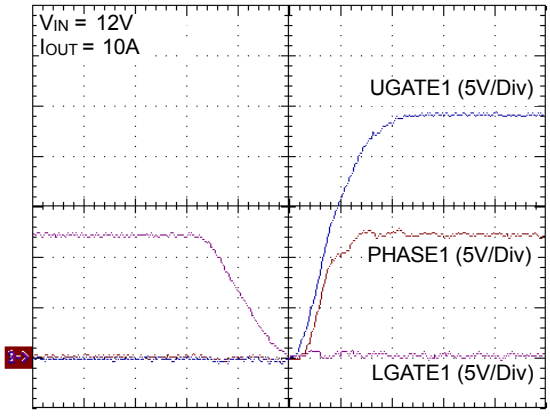
Time (100us/Div)

Dead Time



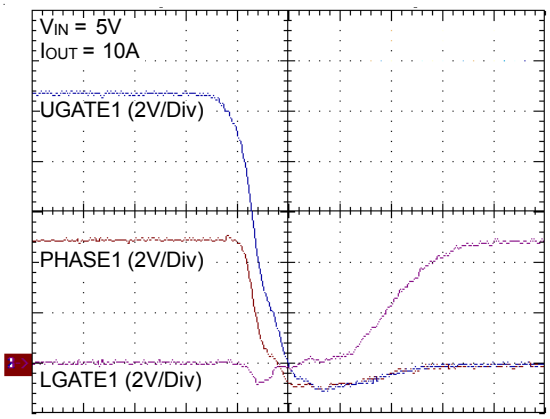
Time (20ns/Div)

Dead Time



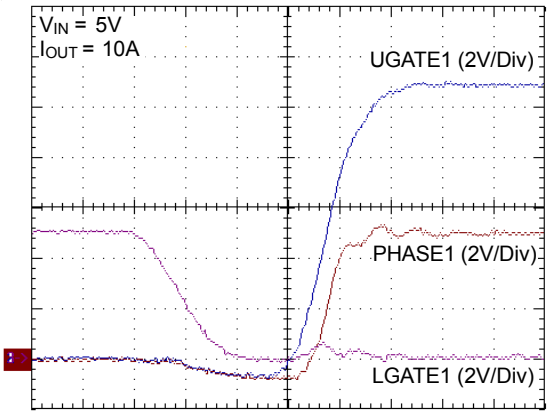
Time (20ns/Div)

Dead Time



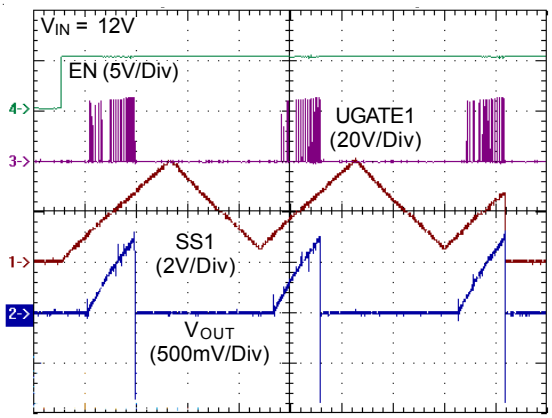
Time (20ns/Div)

Dead Time



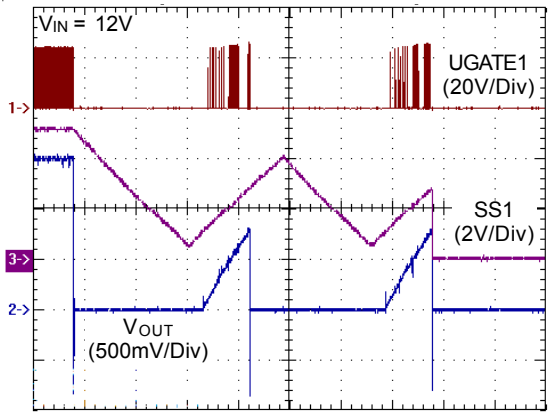
Time (20ns/Div)

Turn On @OCP



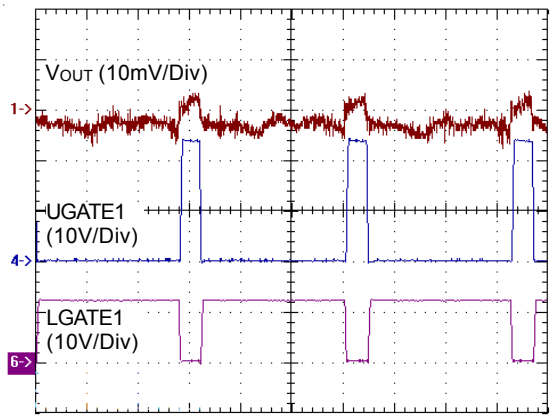
Time (20ms/Div)

OCP



Time (20ms/Div)

Ripple & Noise



Time (1us/Div)

Application Information

Current Sense, Ramp Setting, Current Balance and Current Scaling

RT9256 senses the inductor current through inductor DCR and feeds the current signal back to the control loop. The current sensing circuitry, as in Figure 5 consists of an RC filter, a current sensing GM together with two external resistors. The current flowing the inductor as well as the DCR causes a ripple voltage proportional to inductor ripple current across the equivalent inductor DCR as in Figure 5, The ripple voltage can be obtained using an RC filter in parallel with the inductor, if the component values satisfy the following relationships.

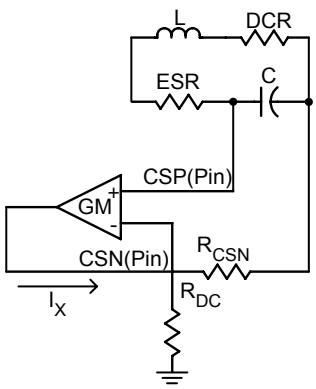


Figure 5

$$\frac{L}{DCR} = ESR \times C$$

The current sense GM converts the voltage drop on the capacitor in the DCR sensing network together with the resistor RCSN connected from the VOUT to the CSN pin. RCSN defines the trans-conductance of the GM stage. An extra external resistor connected from RCSN to GND is recommended to offer the capability of sensing negative inductor current in applications where negative currents are possible at light load conditions. The sensed current Ix is:

$$I_X = \frac{I_L \times DCR}{R_{CSN}} + \frac{V_{OUT}}{R_{DC}}$$, at steady state.

$$I_X = \frac{I_L \times DCR}{R_{CSN}}$$, provided RDC is left opened.

The valley of the sensed current Ix is sampled and held and converted to a DC voltage as a baseline of the current feedback ramp. The sampled and held baseline voltage converted from the sensed current is:

$$V_{XSH} = I_{XSH} \times 24k$$

Where

$$I_{XSH} = \left(I_{OUT} - \frac{0.5\,(V_{IN} - V_{OUT})T_{ON}}{L} \right) \times \frac{DCR}{R_{CSN}} + \frac{V_{OUT}}{R_{DC}}$$

I_{OUT} : output current

V_{IN} : input voltage

V_{OUT} : output voltage

L: inductance value

T_{ON} : on time, T_{ON} = DxTs theoretically, D: duty cycle, Ts: switching clock period.

The external resistor RR is used to sets the internal ramp voltage proportional to current. The simulated ramp voltage is also used to implement the slope compensation set together using a single resistor RR. The relationships between RR and the internal voltage ramp is:

$$\left(\frac{V_{IN} - V_{OUT}}{L} + k\frac{V_{OUT}}{L}\right)\frac{DCR}{R_{CSN}} 24k$$

$$= \frac{V_{IN} - V_{RR}}{RR} \div 64p$$

$$RR = (V_{IN} - V_{RR}) \times \frac{R_{CSN}}{64p} \div \left(\frac{V_{IN} - V_{OUT}}{L} + k\frac{V_{OUT}}{L}\right) \div \frac{DCR}{24k}$$

Where

V_{RR}: the voltage at RR pin to 0.55V

RR : the resistance at RR pin

k : the slope compensation coefficient, which is the ratio of the desired compensation slope to the down ramp slope.

The ramp voltage is summed up with the sensed baseline voltage to form a complete current feedback signal. The simulated ramp signal is fed to the comparator of the PWM modulator, comparing with error amplifier output to generate PWM pulses.

For two-phase mode with single input voltage and equal inductor currents, with the low offsets between internal sensing circuits built in RT9256 and the nature of current mode control loop, perfect current balance can be reached by simply using identical external components.

For the applications in two-phase mode with single input voltage and unequal inductor currents, the valley current ratio between two channels are programmed by setting the ratio of the sensing resistors of these two channels. The relationship of the resistances and the current ratio is:

$$\frac{I_{L1\_VALLEY}}{I_{L2\_VALLEY}} = \frac{R_{CSN1}}{R_{CSN2}}$$

The ramp slope of both channels can be set the same. Note that using unequal currents will cause unequal modulator gain for different channels. Normally, if the current ratio is slightly deviated from 1, compensation should be taken care of for the channel with higher modulator gain, that is, the one with smaller current gain, in other words, the channel with higher current. However, if the current ratio is set too large, the channel with too much slope compensation will move its control loop towards voltage mode.

In two-phase mode with dual input voltages and equal output currents, because the simulated ramp voltage is V_{IN} feedforwarded in RT9256, typically by setting identical RR and R_{CSN} for both channels, balanced modulator gains and inductor currents are automatically achieved. With larger difference in input voltages, the voltage at RR pin, which is around 0.55V, can be taken into considerations as previous calculations for the ramp settings.

In two-phase mode with dual input voltages and unequal channel currents, the ramp setting is the same as that in dual-input, equal output currents conditions, and the current setting consideration is similar to that in single-input, unequal output currents conditions.

Gate control

a. Before SS signal reach the bottom of the ramp voltage, UGATE and LGATE will be off.

b. If EN pin is pulled low UGATE and LGATE will be off.

c. UV protection function caused by FB < 0.6V or V_{IN} < 1.8V will activate the Vin detection mode. In Vin detection mode, the UG LG will be off and SS will be pulled low until ramp setting mode is activated. In two switcher mode, the detection function work independently. In two phase mode, ramp setting mode will be activated when both channel are ready.

d. When OC function occurs and SS > VCC5 – 1.3, a constant current of 10μA starts to discharge the capacitor connected to SS pin right away. When OC occurs, UGATE and LGATE will be off. When the voltage at the capacitor connected to SS pin pass about 0.4V, a constant current of 10uA starts to charge the capacitor. The PWM signal is enable to pass to UGATE and LGATE. In two switcher mode, OCP function is independent monitor. OCP function in two phase mode monitors both channels, either one can activate OCP. If the OC protection occurs three times, OCSD will be activated and shut down the chip.

e. When fault conditions occur or SS < 0.4V, the current sense function will be disable.

Power good

PG = 1 when soft-start voltage >= (VCC5 – 1.3), and no fault conditions.

a. In two-switcher mode, both channels' condition should satisfy.

b. In two-phase mode, only are fault conditions related to SS2, FB2 omitted.

Feedback Loop Compensation

First, the ramp signal applied to the PWM comparator is proportional to the input voltage provided via the VIN pin. This keeps the modulator gain constant when the input voltage varies. Second, the inductance valley current proportional signal is derived from the voltage drop across the ESR of the inductance is added to the ramp signal. This effectively creates an internal current control loop. The resistor connected to the CSN pin sets the gain in the current feedback loop. The following expression estimates the required value of the current sense resistor depending on the maximum load current and the value of the inductance ESR.

$$R_{CSN} = I_{MAX} \times \frac{L_{ESR}}{90\mu A}$$

Due to implemented current feedback, the modulator has a single pole response with -1 slope at a frequency determined by the load,

$$F_{PO} = \frac{1}{2\pi \times R_O \times C_O}$$

where R_O is load resistance and C_O is load capacitance. For this type of modulator, a Type 2 compensition circuit is usually sufficient.

RT9256 is a simulated current mode buck converter using the high gain error amplifier with transconductance (OTA, Operational Transconductance Amplifier)

The Transconductance

$$GM = \frac{\Delta I_{OUT}}{\Delta V_M}$$

The mid - frequency gain.

$$\Delta V_{OUT} = \Delta I_{OUT} Z_{OUT} = GM \Delta V_{IN} Z_{OUT}$$

$$G = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = GMZ_{OUT}$$

Z_{OUT} is the shut impedance at the output node to ground (see Figure 6 and 7)

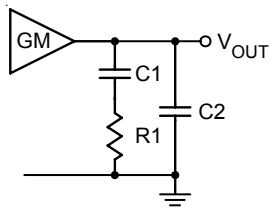


Figure 6. A Type 2 Error Amplifier with Shut Network to Ground

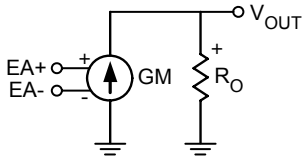


Figure 7. Equivalent Circuit

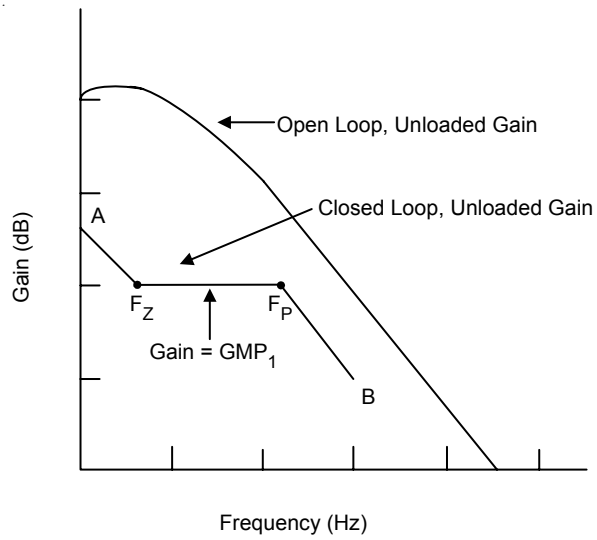


Figure 8. Gain

Figure 8 shows a type two amplifier and its response along with a non-compensated one.

The type two amplifier, in addition to the pole at origin, has a zero-pole pair that cause a flat gain region at frequency between the zero and pole

Pole and Zero :

$$F_P = \frac{1}{2\pi \times R1 \times C2}; F_Z = \frac{1}{2\pi \times R1 \times C1}$$

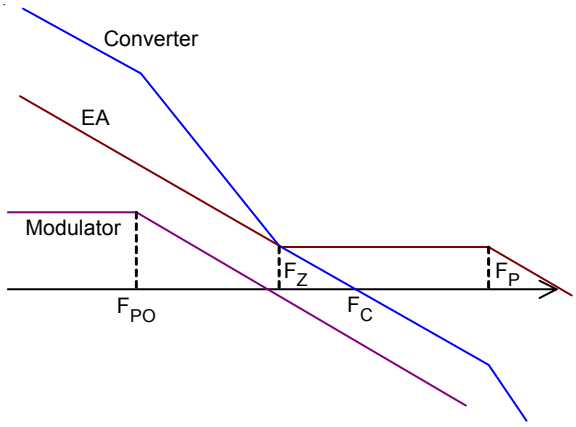


Figure 9. Feedback Loop Compensation

Figure 9 shows the type two amplifier and its response along with the response of the current modulator and the converter.

There is another type of compensation called type three compensation that adds a pole-zero pair to the type two network.

As shown in Figure 10, adding a network between V_{OUT} and V_{FB} in addition to the original type two compensation can result in type three compensation. Figure 11 shows the difference of their AC response. Type three compensation has an additional pole-zero pair that causes a gain boost at the flat gain region.

Pole and Zero :

$$F_P = \frac{1}{2\pi \times [R1//R2] \times C}; F_Z = \frac{1}{2\pi \times R1 \times C}$$

But the gain boosted is limited by the ratio (R1+R2)/R2.

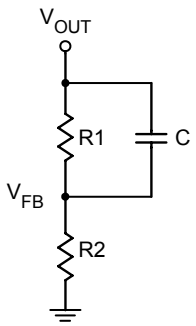


Figure 10. Additional Network of Type Three Compensation Adding at V_{OUT} and V_{FB}

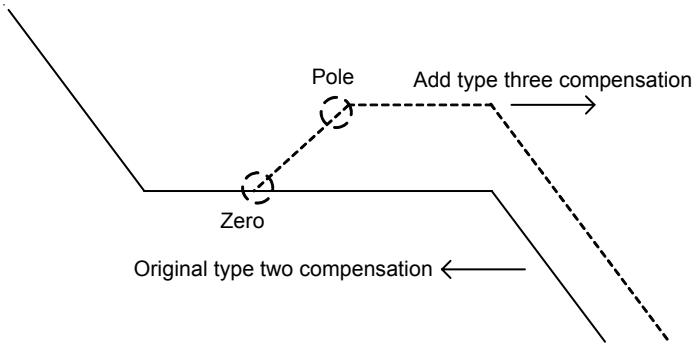


Figure 11. AC Response Curve of Type Two and Three

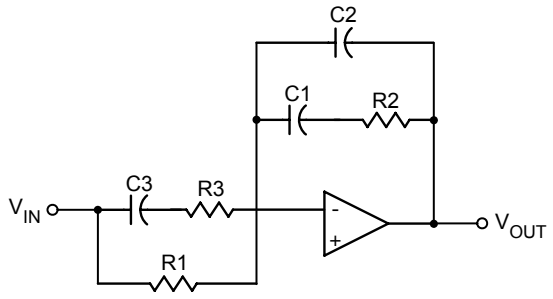


Figure 12. Type Three Compensation Network

Type three compensation can also be done as shown in Figure 12. It has a pole at the origin, two poles, and two zeros.

$$\text{Zero}: F_{Z1} = \frac{1}{2\pi \times R2 \times C1};\ F_{Z2} = \frac{1}{2\pi \times [R1+R3] \times C3}$$

$$\text{Poles}: F_{P1} = \frac{1}{2\pi \times R2 \times C1 \times C2};\ F_{P2} = \frac{1}{2\pi \times R3 \times C3}$$

With small value of R3 and proper chosen poles-zeros, the gain boost will be less limited and obvious than that of the first kind of type three compensation.

Protection

V_{IN} detection

The V_{IN} detection circuitry monitors the switching power source when power up. As V_{IN} > 1.8V, RR pin is enable for ramp setting and the chip is in ramp setting mode. The voltage at RR pin will be about 0.55V. Otherwise, the chip will be in V_{IN} detection mode and RR pin is disable for ramp setting until V_{IN} > 1.8V. In V_{IN} detection mode, the UGATE and LGATE will be off and SS will be pulled low by a constant current of 10uA. The chip will enter the ramp setting mode and SS will re-softstart when V_{IN} > 1.8V. In two switcher mode, the detection function work independently. In two phase mode, ramp setting mode will be activated when both channel' s V_{IN} are ready.

OCP

The RT9256 use cycle by cycle current comparison. The over current level is set by IMAX pin. When OC function occurs and SS > VCC5 – 1.3, a constant current of 10uA starts to discharge the capacitor connected to SS pin right away. When OC occurs UGATE and LGATE will be off. When the voltage at the capacitor connected to SS pin pass about 0.4V, a constant current of 10uA starts to charge the capacitor. The PWM signal is enable to pass to the UGATE and LGATE. In two switcher mode, OCP function is independent monitoring. OCP function in two phase mode monitors both channels, either one can activate OCP. If the OC protection occurs three times, OCSD will be activated and shut down the chip.

RT9256 uses an external resistor R_{IMAX} to set a programmable over current trip point. OCP comparator compares each inductor current with this reference current. RT9256 uses hiccup mode to eliminate fault detection of OCP or reduce output current when output is shorted to ground.

$$\frac{V_{IMAX}}{R_{IMAX}} \Leftrightarrow I_X = \frac{DCR \times I_L}{R_{CSN}} + \frac{V_{CSN}}{R_{DC}}$$

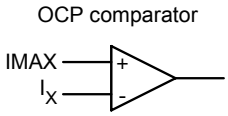


Figure 13

UVP

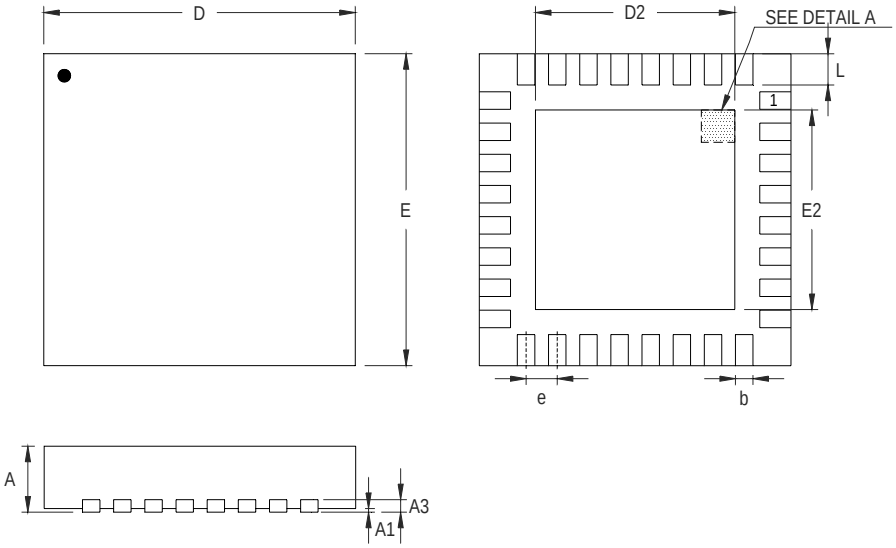
By detecting voltage at FB pin when SS > VCC5 – 1.3. If FB < 0.6, the chip will enter the V_{IN} detection mode. In V_{IN} detection mode, the UGATE and LGATE will be off and SS will be pulled low by a constant current of 10uA. A constant current oh 10uA starts to charge capacitor at SS pin when SS pass 0.4V.

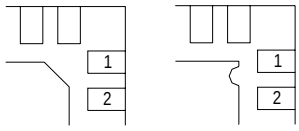
In two switcher mode, the detection function work independently. In two phase mode, ramp setting mode will be activated when both channel are ready.

OTP

Monitor the temperature near the driver part within the chip. Shutdown the chip when OTP.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.500	3.750	0.138	0.148
E	4.950	5.050	0.195	0.199
E2	3.500	3.750	0.138	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 32L QFN 5x5 Package

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